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**HIGH VOLTAGE BIAS WAVEFORM GENERATOR FOR AN RF MEMS
MICROSWITCH**

BY

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THESIS

Submitted to the University of New Hampshire

in Partial Fulfillment of

the Requirements for the Degree of

Master of Science

in

Electrical Engineering

May, 2008

UMI Number: 1454987

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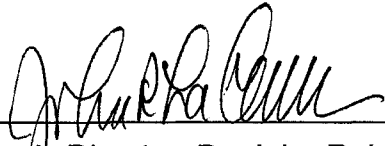
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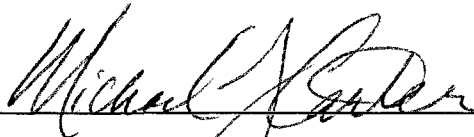
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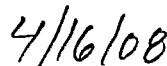
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ABSTRACT

HIGH VOLTAGE BIAS WAVEFORM GENERATOR FOR AN RF MEMS MICROSWITCH

by

James A. Brandt

University of New Hampshire, May, 2008

An integrated high voltage bias driver for a Radio Frequency Micro-Electro-Mechanical System (RF MEMS) microswitch is proposed. The design and implementation in a $0.7\mu\text{m}$ integrated circuit process with high and low voltage transistors is shown along with tested results. High voltage Double-Diffused Metal Oxide Semiconductor (DMOS) transistors in combination with low voltage digital logic provide a non-linear solution that achieves rise and fall times of $1\mu\text{s}$ while keeping power use to a minimum. System design and tradeoffs are presented for alternate approaches and combinations as well as future integration with Direct Current – Direct Current (DC-DC) voltage conversion and an internally generated clock.

CHAPTER 1

INTRODUCTION

The field of Micro-Electro-Mechanical Systems (MEMS), also referred to as micro machines or microsystems, is typically thought to occupy size dimensions from 0.1 micrometers to the centimeter range. Fabrication at these dimensions is typically done with the tools developed for the manufacture of microelectronics [1]. Most of the electrical effects associated with microelectronics, also apply to MEMS with the addition of the mechanical effects such as stress, strain and motion.

Most MEMS systems consist of a sensor or an actuator along with the associated control and processing to make a complete integrated system. Some MEMS sensor systems include accelerometers and gyroscopes used in the aerospace and automotive industries as well as transducers such as microphones. Actuators include microswitches and optical switches used in communications applications as well as display technologies such as the Digital Light Processor made by Texas Instruments. There are also biological applications, using microfluidics for use in genetic analysis and drug synthesis.

Radio Frequency (RF) MEMS switches have been developed extensively in recent years, with a reliable and practical RF MEMS switch having been a longstanding goal for many years now [2]. Both capacitively coupled switches

and Direct Current (DC) coupled switches are possible. The applications of RF MEMS capacitive switches include any RF areas that need efficient signal routing. High volume applications such as cell phone Transmit / Receive (T/R) switches might be possible allowing for single chip integration on silicon with better performance than current solid-state methods. Comparisons between Field Effect Transistor's (FET's), Positive Intrinsic Negative (PIN) diodes and RF MEMS switches have been made that show RF MEMS switches have considerable advantages in isolation, loss and distortion[2]. Other possibilities for RF MEMS switches in communication and radar systems applications include tunable filters, phase shifters and reconfigurable antennas.

The goal of this research was to show that an integrated solution to the control and generation of the high actuation voltages needed to operate the switch was possible. This may make it possible in the future to combine the control circuitry into the existing MEMS process, leading to a complete system solution. Multiple analog and digital approaches were investigated and considered, as well as multiple levels of integration, including driving one or several RF MEMS switches, and onboard DC-DC conversion. Ultimately a design that integrated only the high voltage switching and low voltage control logic was chosen and implemented. The circuit was manufactured in the 0.7 μ m AMI Semiconductor I2T100 integrated high and low voltage process [3].

Chapter 2 presents a technology overview of the RF MEMS switch and system considerations in its operation as well as high voltage integrated circuits and the I2T100 process. Chapter 3 covers in depth the bias voltages,

power and other requirements for a bias system. Also different top down system designs are discussed with there associated trade-offs. Chapter 4 contains the system design while Chapter 5 presents the layout, simulation and testing results. Conclusions, design modifications and future work are presented in Chapter 6.

CHAPTER 2

TECHNOLOGY OVERVIEW

Several technologies need to be understood before approaching the circuit design of a bias generator. The first technology is that of the RF MEMS capacitive switch itself since this is the device that the bias generator will operate. The second topic is the coupling of the bias generator circuitry to the RF MEMS switch and the system implications of the combination. The third is the operation and construction of silicon devices that will support large voltages and are usually grouped together under the high voltage integrated circuit (HVIC) and power integrated circuit (PIC) categories, the high voltage active component of which is usually referred to as double-diffused metal oxide semiconductor (DMOS). A combination of these basic technologies together will allow for the creation of a complete RF MEMS switch system.

2.1 RF MEMS Capacitive Switch

The particular device that the bias generator was designed to drive was developed at the Massachusetts Institute of Technology Lincoln Laboratory (MITLL) Advanced Silicon Technology group [4]. The switch contact is capacitively coupled through an oxide layer. Thus the passable frequency range is from 5 GHz to at least 40 GHz. As shown in Figure 2.1.1 and Figure 2.1.2, the

RF MEMS capacitive switch is constructed of a tri-layer membrane consisting of aluminum that is sandwiched between two layers of silicon dioxide. By using two different stresses on the top and bottom, the cantilever naturally tends to curl upward. When curled up, there is a relatively large air gap between the in and out terminals, which presents a high RF impedance. A third terminal, or pull down electrode, is buried beneath the oxide layer directly under the switch. When a DC voltage is applied, there is electrostatic attraction between the cantilever and the pull-down electrodes, which causes the switch to flatten out and press down on the oxide layer on the RF output pad.

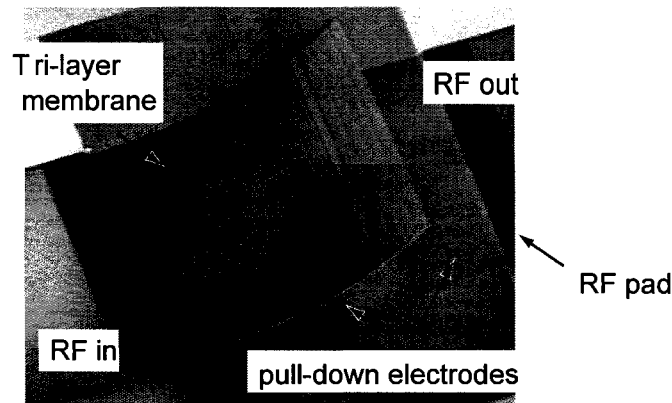


Figure 2.1.1 Scanning Electron Micrograph of an RF MEMS Switch [5]

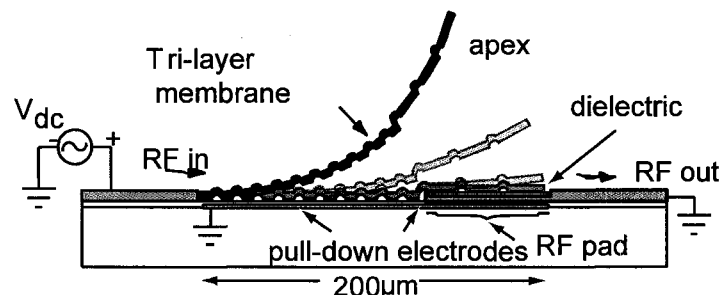


Figure 2.1.2 - Graphical Display of an RF MEMS Switch Operation [5]

A model of the load of the RF MEMS switch to the bias circuit can be made by considering just the capacitance in the down state. This is shown

symbolically in Figure 2.1.3. This is a simplified worst case model of the switch since a more complete model would account for the fact that the up state capacitance is several orders of magnitude less and variation would occur as the switch opens and closes. This large variation in capacitance has also been exploited to make a tunable varactor [6]. In order to activate the switch a DC voltage on the order of 40-80V should be applied between the A and B terminals shown in Figure 2.1.3. After the switch closes, a lower voltage can be applied between VA and VB as well as between VA and VC to hold the switch down securely. A more complete description of actuation and operational voltages is covered later in Section 3.1.

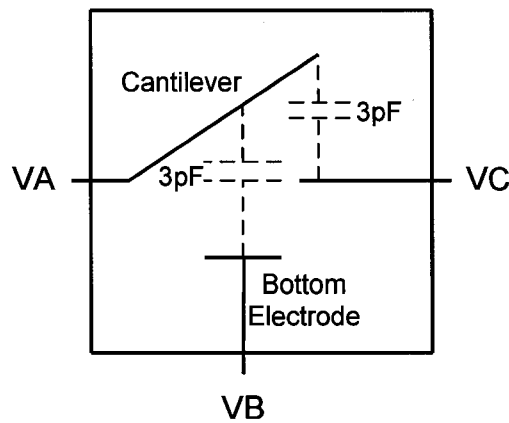


Figure 2.1.3 - RF MEMS DC Electrical Properties

The RF operating performance of the switch has been tested. Hot switching levels of 1.7 Watts (32.3 dBm) as well as cold switching levels of 10 Watts (40 dBm) have been reported [5]. In conjunction with a wide-band packaging technology also developed at MITLL[7], insertion loss of 0.11dB with better than 19 dB isolation at 20 GHz have been reported [8]. The packaging

technology also allows multiple switches to be packaged into series-shunt and SP4T configurations that allow for greater isolation.

2.2 RF MEMS System

To make an integrated system, the high voltage bias waveform needs to be generated automatically. Thus a bias generator should control the switch and allow it to be operated with only a Transistor-Transistor Logic (TTL) signal. A basic block diagram of this system is shown in Figure 2.2.1. The bias generator controls all three terminals of the switch in the DC domain. The switch terminals are connected through high impedance connections to the bias generator so the RF performance is not affected. A complete system might also include a monitoring system that would measure and compare the RF power in and out of the switch and provide a feedback control signal to the bias generator, although this is beyond the scope presented here. With a feedback signal, the actuation voltages could be adjusted to maximize the switch RF performance. Mechanical stress during the switch lifetime could also be minimized by running the actuation voltage at the minimum, while still maintaining good RF performance. Compensation for manufacturing variations could also be accommodated.

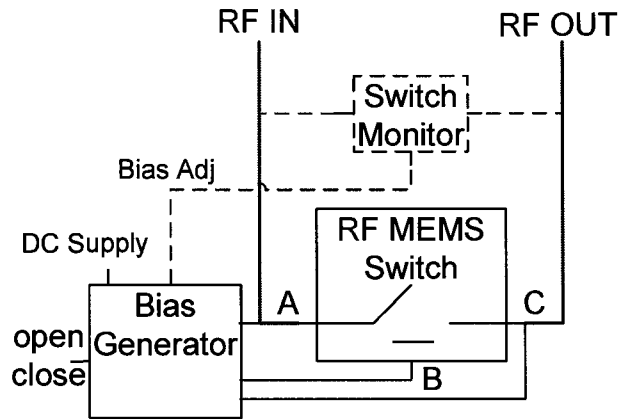


Figure 2.2.1 - Block Diagram of Basic RF MEMS Switch System

2.3 High Voltage Integrated Circuits

HVIC and PIC's have been envisioned since the development of high voltage silicon MOSFETS in the late 1970's. The only noticeable difference between an HVIC or PIC is in the power or current handling capacity. The differentiation between an HVIC or PIC and standard integrated power electronics is the extra integration of standard low voltage CMOS transistors and their higher voltage counterparts on the same wafer. DMOS style transistors are the most widely used high voltage devices in silicon technology. They were originally developed as individually packaged standalone transistors for high power applications and have been widely deployed in many applications such as cell phone base station transmitter amplifiers, class D switching amplifiers and switching power supplies [9]. In order to facilitate integration with other devices, the lateral DMOS (LDMOS) has also been developed. Electrical operation is the same, but the drain location is moved from the substrate to the top of the wafer.

A DMOS transistor's operation is significantly different from that of the typical MOSFET. The most notable difference is the fact that it is a unidirectional

device with current flow from source to drain and not vice versa. As shown in Figure 2.3.1, DMOS transistors operate like a standard MOSFET with a channel region formed under a gate oxide. Unlike a standard transistor, the channel region is connected to the drain via a lightly doped region typically called the drift region. This structure puts a reversed biased diode in line with source and drain and thus supports a large voltage at the drain without punch-through occurring as happens in standard MOSFET transistors[10]. The LDMOS operates in essentially the same way, but the drain has been moved to the top of the wafer as shown in Figure 2.3.2. This allows integration but also consumes a larger area. The LDMOS operation is limited by the breakdown voltage of the drift region to substrate. In many cases silicon on insulator technology or localized buried layers (insulators) are used to support large voltages.

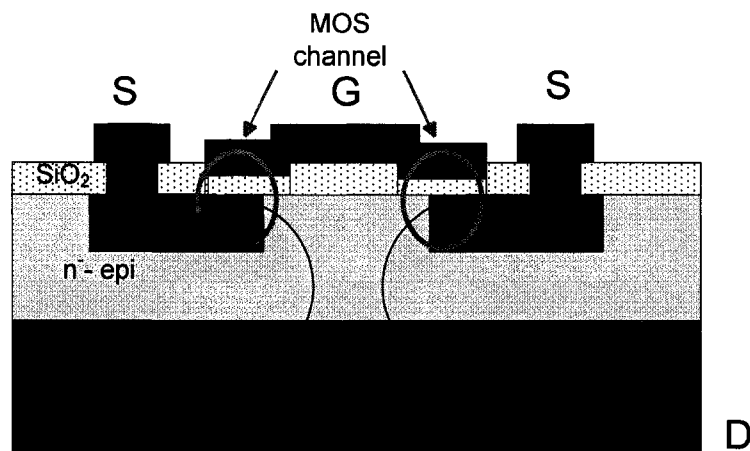


Figure 2.3.1 - DMOS Cross Section

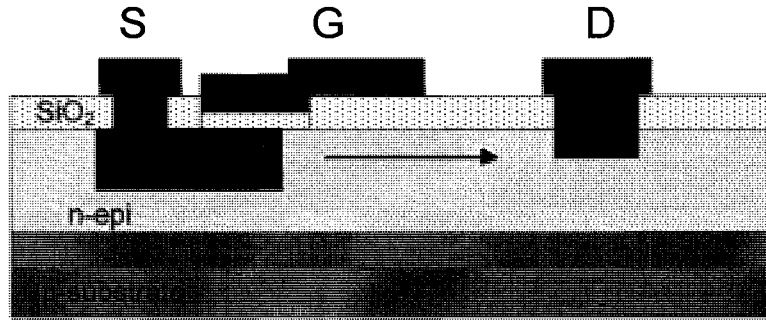


Figure 2.3.2 - LDMOS Cross Section

Although many semiconductor companies manufacture integrated HVIC style processes, most of the processes readily available for prototyping or multi-project runs do not meet the minimum voltage requirement of 80 V. A quick listing of multi-project runs is shown in Table 2.3.1. The shaded MOSIS runs are the most available and run frequently, thus making them a good choice. The I2T100 process is available through MOSIS [11].

Table 2.3.1 - HVIC Multi-project Runs Available

	Company	Feature Size (μm)	Voltage (V)
MOSIS	AMI Semiconductor	.7	100
	AMI Semiconductor	.35	80
	TSMC	.18	32
	Austria Microsystems	.35	50
	DALSA Semiconductor	.8	300
	ATMEL	.35	40
	Jazz Semiconductor	.25	12
	Jazz Semiconductor	.5	40
	Chartered Semiconductor	.18	32

The I2T100 process consists of both high and low voltage transistors which can be floated above the substrate on a buried layer. Generic cross sections of the floating version of the n-style LDMOS (FNDMOS) and p-style LDMOS (FPDMOS) are shown in Figure 2.3.3 and Figure 2.3.4 respectively. A more detailed description of the process can be found in [3] and [12]

To float the FNDMOS, a large lightly doped n-type region, called the NTUB, is created through implantation on top of a localized insulating or buried layer. The p-type channel material is then created as the PBODY. An n-type source is created in the PBODY as well as an n-type contact. The n-type drain contacts complete the transistor with the drift region formed between the drain contact region and the PBODY. The FPD MOS is created in a similar manner except the NTUB is not added around the channel area. Many PNP and NPN transistors are also available with the NTUB and PBODY allowing the formation of lateral bipolar structures and high voltage diodes [3].

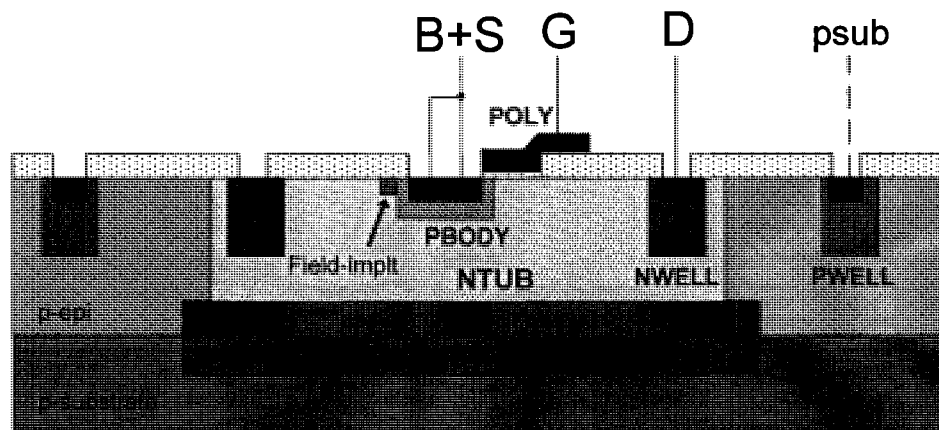


Figure 2.3.3 - Generic I2T FNDMOS Cross Section

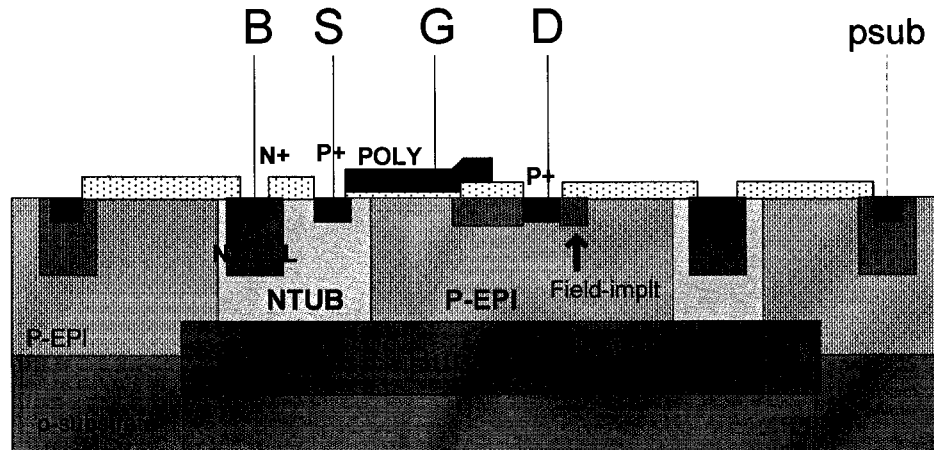


Figure 2.3.4 – Generic I2T FPD MOS Cross Section

The process also includes passive components such as high, medium and low ohmic poly resistors. Two poly layers and three metals are available along with several types of capacitors depending on the desired voltage range. Capacitors based on a standard MOS transistor capacitance have large capacitance to area ratios $1.97 \text{ (fF}/\mu\text{m}^2\text{)}$, but are limited to the 5 V supported by the gate oxide. Versions based on the DMOS transistors are also available with $0.812 \text{ (fF}/\mu\text{m}^2\text{)}$, and voltages up to 12 V. A poly0-poly capacitor with $0.345 \text{ (fF}/\mu\text{m}^2\text{)}$, allows a 30 V range and a poly0-metal1-metal2 stacked capacitor with $.091 \text{ (fF}/\mu\text{m}^2\text{)}$, will allow 100 V operation.

Silicon DMOS transistors are the most logical technology to control silicon MEMS switches. They provide the ability to manipulate higher voltages than traditional CMOS transistors. HVIC and specifically the I2T100 process provide the ability to combine the low power operation of standard CMOS with the high voltage capability of DMOS in one manufacturing process. The I2T100 process also provides many different active and passive devices allowing a flexible design approach.

CHAPTER 3

SYSTEM AND BIAS CONTROL OPERATION

This chapter presents detailed requirements and design options for the bias driver. The high voltage waveform needed for switch actuation is discussed in 3.1. The capacitive loading and its implications are also discussed as well as power and efficiency parameters. Section 3.2 presents a top-down view of different design choices, analog vs. digital, that could be made when considering a single switch. Section 3.3 covers design choices that could be made in the high voltage section of the design. Section 3.4 expands upon the other design sections to discuss options when considering a bias driver for multiple RF MEMS switches.

3.1 Requirements

The ideal requirements of a bias generator would be that it is integrable on the same wafer as the switch or that it is easily bonded within the RFMEMS package so as to create a single system. It also needs to be able to handle high voltages and be able to drive a capacitive terminal of approximately 3 pF high or low within approximately 1 μ s. The needed voltages / waveform should be generated given only a standard logic (TTL) input and DC power. Power consumption must be extremely low with minimal to no power consumed when the RF MEMS switch is in a fixed state.

The DC bias waveform needed to operate the RF MEMS microswitch is shown in Figure 3.1.1. The voltages shown are all differential in nature across the capacitance of the switch as was shown earlier in Figure 2.1.3. The rise and fall times between these should all be in the 1 μ s range. The waveform can be divided into two different operations. The first is typically referred to as the “pull-down” and starts with a large voltage or “kick” of approximately 80V between terminal A and B, to get the cantilever moving. As it starts to move, the voltage is reduced to approximately 60V as the cantilever is pulled down into contact with the RF output pad, previously shown in Figure 2.1.2. The kick duration is approximately one half to one fifth that of the total time needed to pull the cantilever down. VA-VC should be zero or a low voltage (under 20 V) during this whole transition; thus terminal C needs to track terminal A.

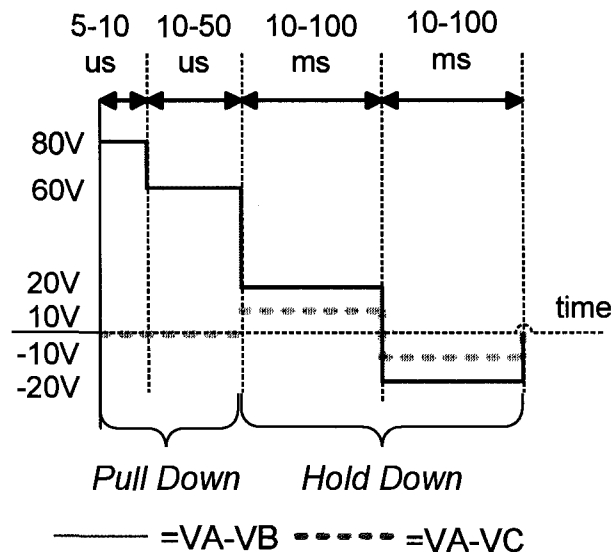


Figure 3.1.1 - RF MEMS Microswitch Bias Waveform

The second operation is typically referred to as “hold-down” and begins after the cantilever makes contact with the RF output pad. A voltage of 20 V between terminal A and B is typically sufficient, while VA-VC should be

approximately one half this, so that the cantilever is held firmly down without causing breakdown through the thin oxide on the RF output pad. V_A-V_B and V_A-V_C then needs to flip from positive to negative to keep the charge from dissipating and thus the electrostatic force lessening, allowing the cantilever to rise. The transition between these flips is very important and must be at or below the 1 μ s range to keep the cantilever from momentarily releasing up. The duration of each hold-down pulse is much longer (greater than three orders of magnitude) relative to the pull-down operation.

To keep the operation of the switch normalized and to keep charge buildup or trapping from occurring on the RF MEMS switch cantilever, the waveform polarity must be alternated every other switching cycle. As shown in Figure 3.1.2, the differential voltage or terminal order is reversed on the second closing of the switch as opposed to the first. In terms of the terminal voltages, the reversed polarity introduces some differences. Terminals A and B are simply interchanged, while terminal C must still follow terminal A.

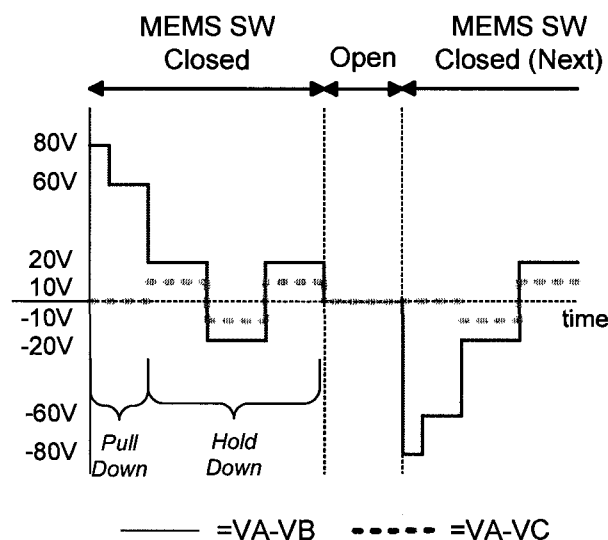


Figure 3.1.2 - Alternating RF MEMS Bias Waveform

The ideal bias waveform generator should also be able to control duration and voltage levels at all three terminals, thus allowing complete modification of the waveform and precise control of the switch over process and lifetime. As shown in Figure 3.1.1, the duration of the kick voltage and pull-down voltage should be independently adjustable to be able to accommodate RF MEMS switches with varying mechanical properties. The hold-down voltage should also be adjustable to allow for these variations so that the switch can be held firmly without having to compressively overstress the oxide on the RF output pad. Ideally, all voltage levels could be varied independently as well.

Differences in the way the terminals are driven can have a large effect. Consider the general cases of an amplifier, either linear (op-amp) or non-linear (digital inverter), driving an ideal load that is either purely capacitive or resistive. For a positive voltage pulse, there will be a differing current response depending on the load. For a resistive load, the current waveform mimics the voltage pulse as shown in Figure 3.1.3. This is a familiar response that follows directly from Ohm's Law. Now consider the same voltage pulse with a capacitor as the load. The current response, shown in Figure 3.1.4, is now just a positive spike that occurs as the capacitor charges as well as a negative spike as it discharges. These two different current responses influence the design of the driver.

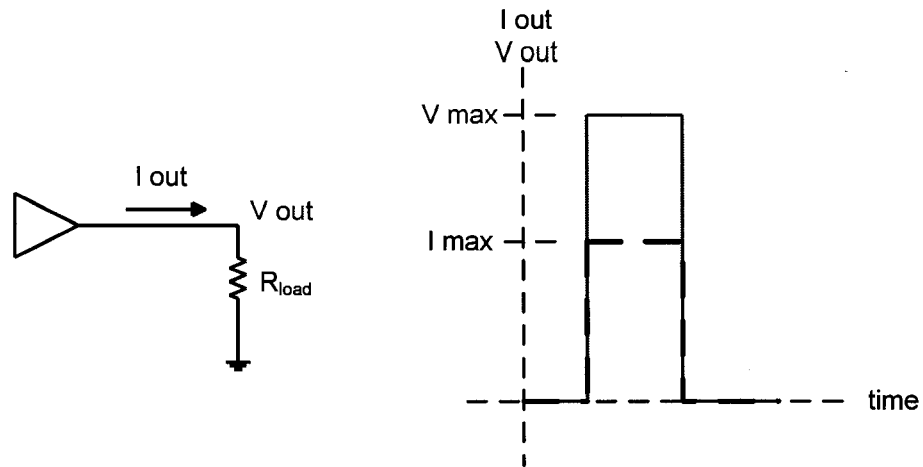


Figure 3.1.3 - Positive Voltage Pulse with a Resistive Load

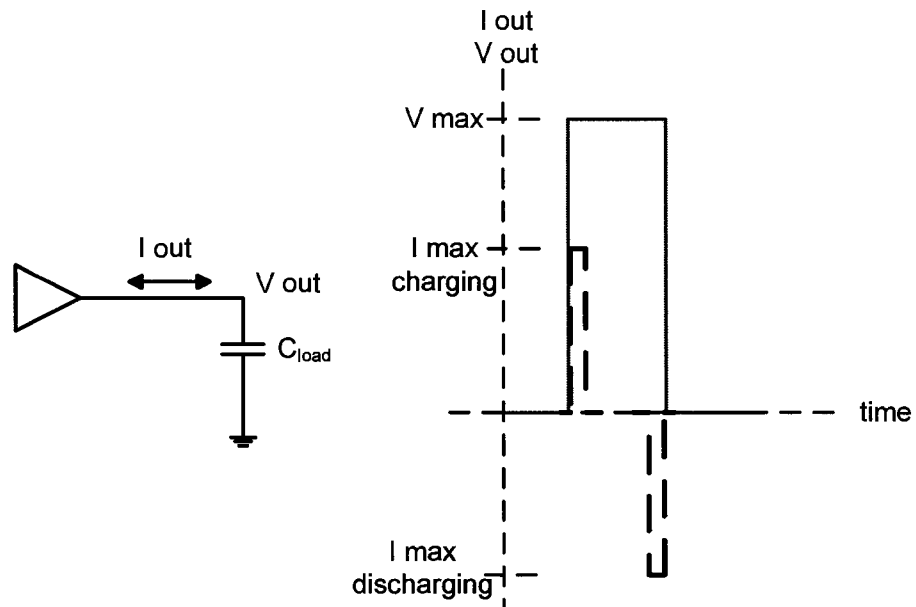


Figure 3.1.4 - Positive Voltage Pulse with a Capacitive Load

The RF MEMS switch terminals represent the case in Figure 3.1.4. Any circuit designed to drive the DC bias of the switch must have a bidirectional current flow. The switch terminals will absorb current as the DC bias is turned on and return it as it is turned off. Remember that from section 2.3, the current in an LDMOS is unidirectional and thus can not be used individually to source a

voltage to one of the switch's terminals. This requirement becomes important as different driver circuits are considered later on.

Power consumption is also a requirement since the RF MEMS switch has direct low power applications. To be competitive with current technologies, it must have comparable operating power. As a first comparison using the simple model introduced in Figure 2.1.3, the ideal power consumed by the switch was calculated (Appendix A) and the results of which are shown in Figure 3.1.5 plotted against switching frequency with variations in duty cycle. The duty cycle variation is due to the fact that there is differing amounts of power consumption during the pull-down and hold-down of the switch. For relatively low switch cycle times (less than 1 Hz), the duty cycle dominates power consumption as there are many more hold-down flips in polarity occurring than there are pull-down occurrences. As the switch activity increases, the pull-down power begins to dominate.

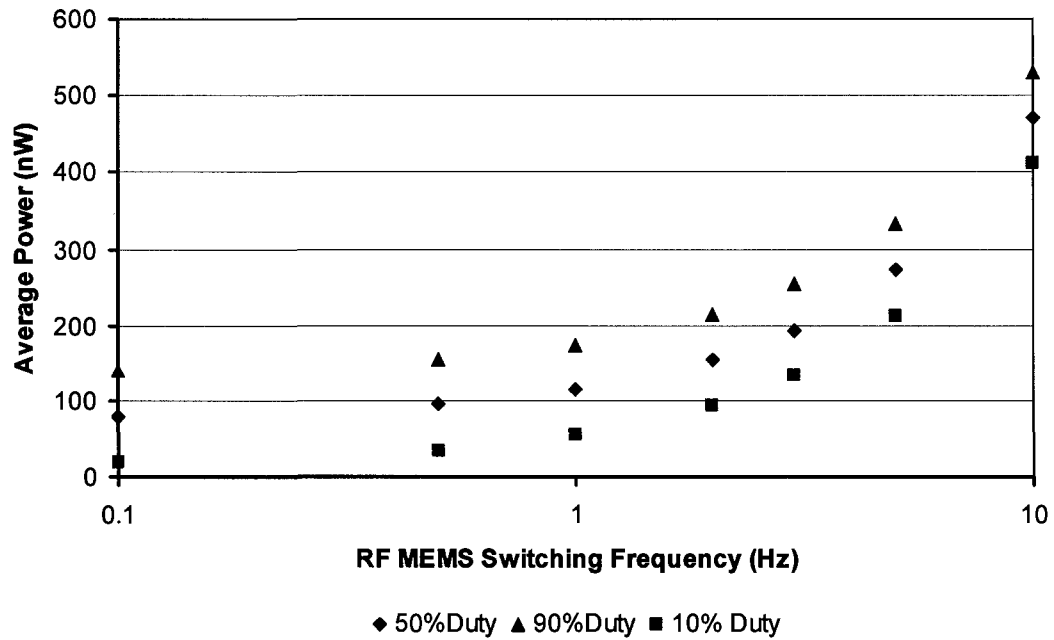


Figure 3.1.5 - RF MEMS Switch Average Power Consumption

A good reference power is at a 50 % duty cycle and 1 Hz giving a power consumption of approximately 120 nW. A bias circuit that consumed several hundred nanowatts would give an efficiency of approximately fifty percent.

Dividing the power by the voltage range of the bias circuit (20-80 V) gives bias currents up to ten nanoamps. These power and current levels are very hard, if not impossible, to achieve in an HVIC process that is optimized for high power.

The real question of appropriate power consumption then becomes a comparison of the system of the RF MEMS microswitch and bias generator versus other technologies already used in industry (Gallium Arsenide transistors (GaAs) switches or PIN Diodes). In Table 3.1.1 a selection of commercially available RF switches are presented. From this perspective an operating power of several milliwatts would be a good comparable level. As discussed in Section 2.1, the RF

MEMS switch has comparable or significantly better RF performance than any of the switches listed here.

Table 3.1.1 - Commercially Available RF Switches

Company Model	Switch Type	RF Frequency (GHz)	Operating Power (mW)	Insertion Loss (dB)	Return Loss (dB)	Max RF Life
MACOM/ MA4SW110	SPST (PIN)	6-20	24-75	.7-1.2	55-42	30
MACOM/ MASWGM0002	SPDT (GaAs)	2-20	15.6-48	2.5-4.3	54-37	31
Skyworks/ AS165-59	SPST (GaAs)	.7-2.5	1 – 1.4	.7-1.2	45-38	30
Hittite/ HMC-C019	SPST (GaAs)	0-20	14-17.5	2.3-9	115-60	27

3.2 Single RF MEMS Switch System Design

If only a single RF MEMS switch is considered, a top-down view of the bias system allows an overview of the possible circuits and pieces that need to be designed. A very basic system might look something like Figure 3.2.1. Here the switch is generically interfaced through a high-voltage (HV) system to a generic digital system that will generate and control the bias waveform. Inputs might include a digital signal representing the opening or closure of the switch, a digital as well as HV power source, and a clock source. The RF input and output are shown for illustrative purposes. A more complete system is shown in Figure 3.2.2. Here the clock is internally generated from a ring oscillator or other circuit design. The HV supply is also internally generated by some sort of DC-DC converter that could be integrable into the chip. This could be a charge pump or, with some external components, a Buck-Boost type of design.

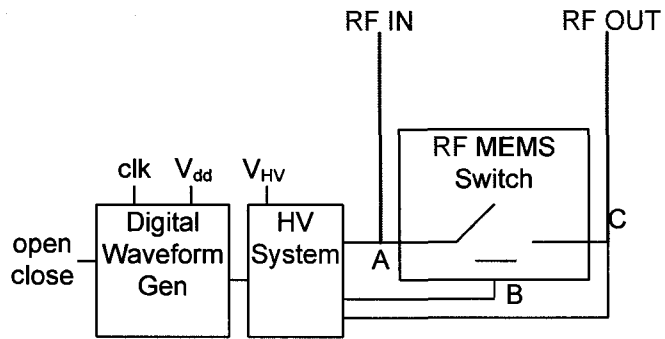


Figure 3.2.1 - Basic RF MEMS Microswitch Bias System

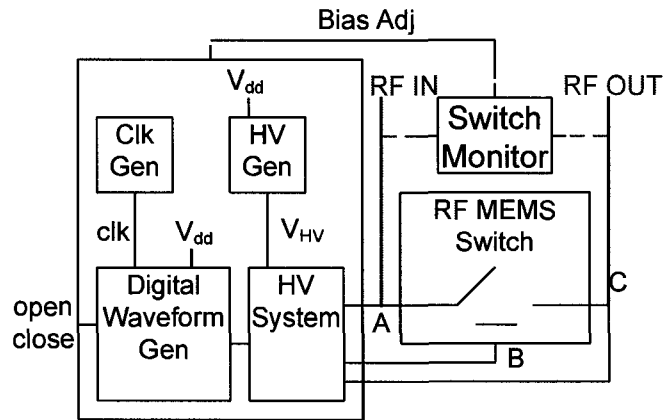


Figure 3.2.2 - RF MEMS Microswitch Bias System with Feedback Control

3.3 High Voltage System Options

An op-amp solution to the HV system of the MEMS driver would allow for the most flexibility in terms of varying the voltages applied to the MEMS switch. If combined with a digital-to-analog converter (DAC) and a micro-processor (μ P) or some other basic digital control, a complete system could be assembled as shown in Figure 3.3.1. This would be a relatively straight forward design and require only one HV power supply.

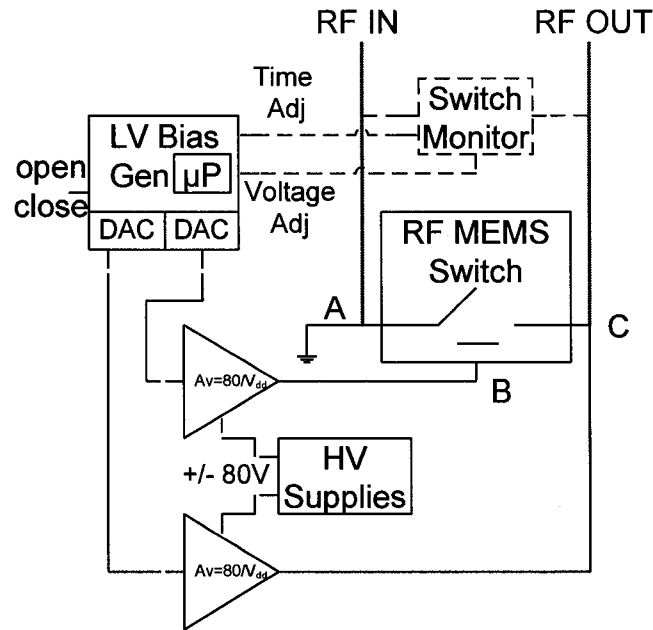


Figure 3.3.1 - RF MEMS Switch and Analog Driver System

Problems would occur when trying to design high voltage op-amps that meet the necessary voltage and speed requirements. The slew rate must be faster than the needed rise time of $1\mu\text{s}$, and thus the required bandwidth will be greater than 1 MHz. Thus, for an 80 V transition, the slew rate would be $80\text{ V}/\mu\text{s}$. To change TTL levels to HV levels it must have a stable gain of at least 16 V/V. This gives a gain bandwidth product greater than 16 MHz. This slew rate and gain bandwidth would be difficult to achieve in a high voltage CMOS process, where DMOS transistors are constrained by long channel lengths, low gain, and large drain resistance. Several high voltage op-amp designs are described in [12] that show this difficulty with slew rates of only several volts per microsecond and a gain bandwidth approaching only 2 MHz. A large standby power of several milliwatts is also reported.

Power consumption would only increase as the op-amp design became faster to meet these design requirements. The op-amp solution also would have

the consequence that there would be a quiescent current necessary during the open state of the MEMS switch. Op-amps available today that can meet the system requirements, such as the Burr-Brown 3584 or the MSK 601, both of which employ a mix of CMOS and bipolar transistor design, have quiescent current requirements of 6.5-15 mA at voltage levels of nearly 100 V. This power loss is too high to be considered for an integrated driver. An all CMOS design, like the Supertex HV254, has a lower operating power, but only a 3 V/ μ s slew rate, making it too slow for an integrated driver. See Appendix B for more information on commercially available technologies.

A digital system would provide less flexibility in terms of variability of output voltages, but would allow a much simpler and more power efficient design. A basic digital system would look like Figure 3.3.2. Here a digital switching driver would be powered by multiple power supplies and drive the RF MEMS switch from only a TTL input signal. The digital bias generator is expanded upon in Figure 3.3.3. Here the waveform timing is controlled by a simple digital circuit that generates signals to turn on the appropriate high voltage switch. These signals are then shifted up to the appropriate voltage to actuate the high voltage switch, typically a PDMOS transistor type. If more integration were desired the HV power supplies could be integrated onto the chip using DC-DC conversion methods such as charge pumps or buck-boost style converters.

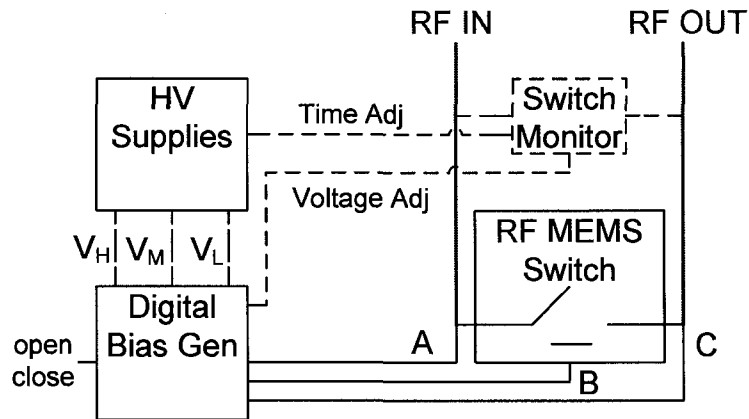


Figure 3.3.2 - RF MEMS Switch and Digital Driver System

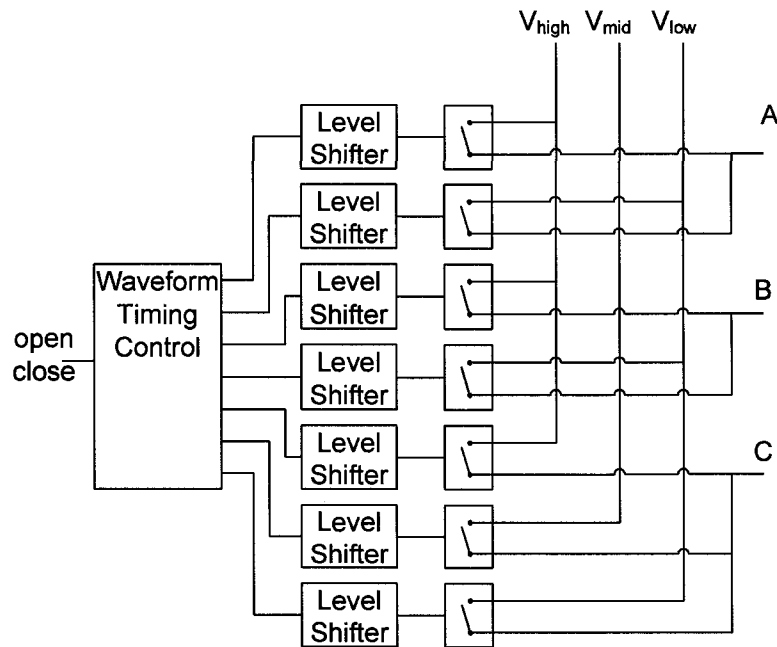


Figure 3.3.3 - Digital Bias Generator

If the DC-DC converters were thought of as the drivers themselves instead of as the power supplies, a mixed signal type of driver like the one shown in Figure 3.3.4 could be designed. A standard digital control is still used, but the charge pumps are now dynamically controlled to raise the low voltage V_{dd} level up to the desired output level in the one microsecond time frame. This would require DC-DC converters with a feedback regulated output and relatively fast

charging operation. This design, while feasible, would require a very large area if charge pumps were used, or many external components if Buck-Boost converters were used. A discussion of DC-DC converters is included in 0. In addition to the size of the charge pumps, they would also need to be able to pump the voltage up or down. A novel bidirectional design can be found in [13].

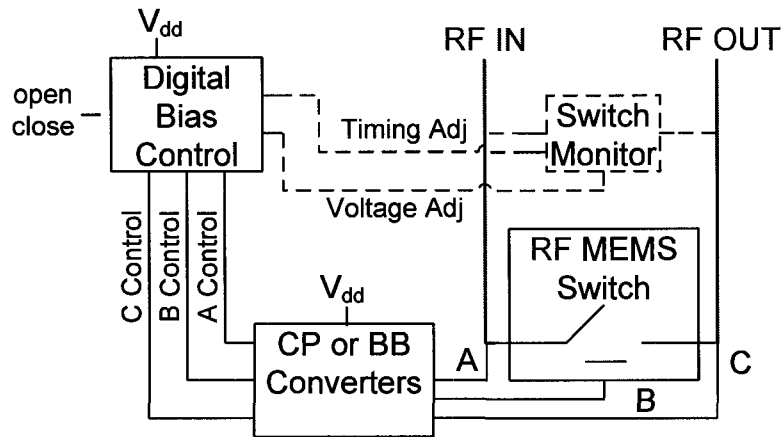


Figure 3.3.4 - RF MEMS Switch and Mixed Signal Driver System

3.4 Multiple RF MEMS Switch System Design and Options

If multiple MEMS switches were to be controlled from a single driver, many design savings could be realized. Figure 3.4.1 shows a basic system with multiple drivers and MEMS switches. The first savings occur by sharing the clock generator and high voltage power supplies. If the drivers are integrated together, more savings can be realized in the low voltage section by integrating the control of the switches as shown in Figure 3.4.2. The added benefit of integration is that there can also be added control over the operation of each MEMS switch relative to the others, thus allowing preprogrammed patterns and variable timing. If an analog approach to the high voltage driver is taken, there is not much more that can be saved by integrating the high voltage sections. Each driver still needs to

have the same number of DAC's and op-amps to allow individual control of each MEMS switch. Integrating a digital driver provides fewer benefits and, if individual control over each MEMS switch is wanted, multiple HV supplies or DC-DC converters would be needed for each RF MEMS switch that is attached to the driver.

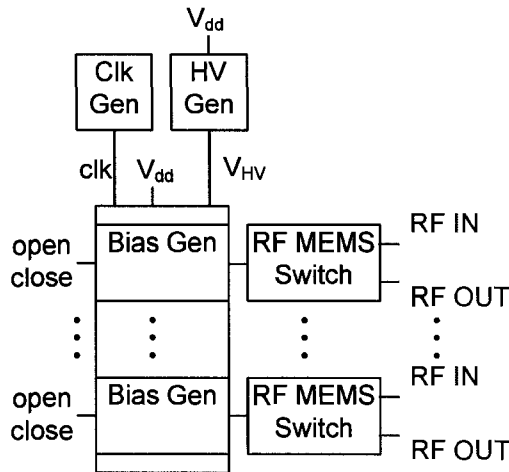


Figure 3.4.1 - Basic Multiple RF MEMS Switch system

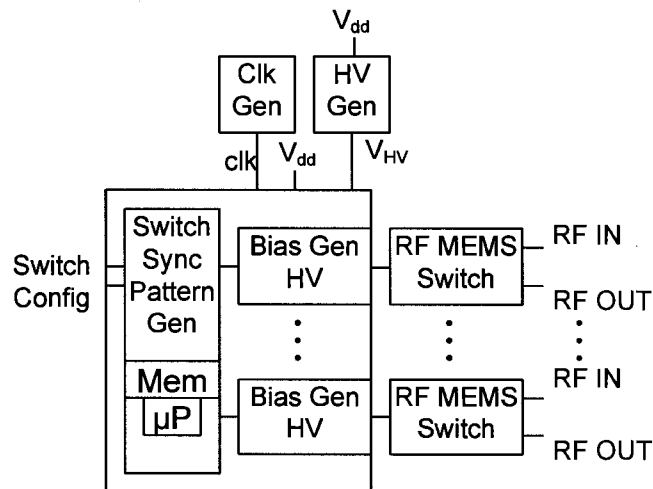


Figure 3.4.2 - Multiple RF MEMS Switch, Integrated Digital Control

If a driver is created with both analog and digital components, it could be possible to save resources in the high voltage sections. In Figure 3.4.3 an op-amp is used to drive a HV analog multiplexer. Such a multiplexer could be made

with a HV switch proposed in [14]. Here a trade-off is made by giving up individual control of each MEMS switch in exchange for less driver area and power. Each switch is still able to be individually either open or closed, but transitions between open and closed configurations can only occur in unison with all switches being effected during any transition. The same trade-off is made in terms of the voltages applied to each MEMS switch, that is no individual control is possible.

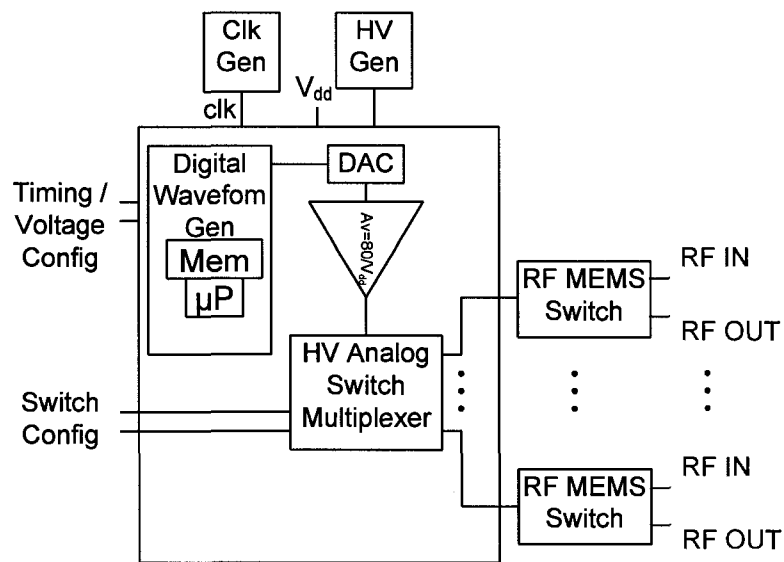


Figure 3.4.3 - Multiple RF MEMS Switch, Combined Analog and Digital Driver

CHAPTER 4

DIGITAL BIAS WAVEFORM GENERATOR DESIGN

This chapter presents the design of the digital RF MEMS switch bias driver that was implemented. Section 4.1 presents a top-down overview of the design. Section 4.2 presents the development of the level shifter by reviewing several more common designs and modifications that lead to the final design. Section 4.3 presents the design of the digital control while Section 4.4 presents the level shifter drivers and the glue logic needed between the waveform generator and the high voltage switches.

4.1 System Overview

The digital bias generator system has four main parts as shown in Figure 4.1.1. The waveform generator consists of low voltage semi-synchronous logic with a clock and logical open/close signal inputs. The outputs are also low voltage, one for each possible high voltage on each terminal. Control signals are generated so that opposite polarity pull-down and hold-down states are created from the last generated pull-down and hold-down state. The override mux is a simple array of standard two to one multiplexers that allow the generator to be overridden. This acts mainly as a testing structure, allowing the low voltage and high voltage parts of the chip to be tested individually. The third section consists

of the low voltage drivers that control the gate functionality of the high voltage switching transistors as well as some extra low voltage glue-logic. The glue-logic generates a signal to ground a terminal if no high voltage is applied as well as keeps track of the terminal C to A tracking needed in the pull-down phase so as to not to overload the RF MEMS switch oxide.

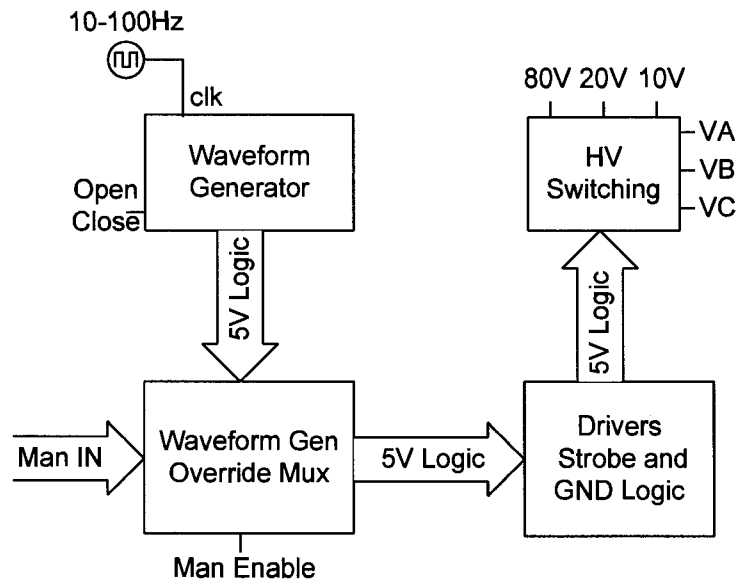


Figure 4.1.1 - Digital Bias Waveform Generator Block Diagram

The HV switching section contains only high voltage circuits and elements. A more detailed block diagram of this section has been included as Figure 4.1.2. Each HV SW (switch) consists of PDMOS transistors that have their gates controlled from ground state logical levels (0-5V) via a level shifter. For each of the three output terminals (VA, VB, and VC), several HV SW elements are ganged together with diodes to prevent reverse voltage biasing from occurring. Each voltage level necessary at any terminal can be switched to the output terminal using just a standard logic signal. The high voltage NDMOS transistor

can be controlled from standard logic levels for grounding each terminal. By controlling these switches appropriately, differential voltages between terminals A-B and A-C can be generated that resemble the required voltages previously shown in Figure 3.1.1 and Figure 3.1.2.

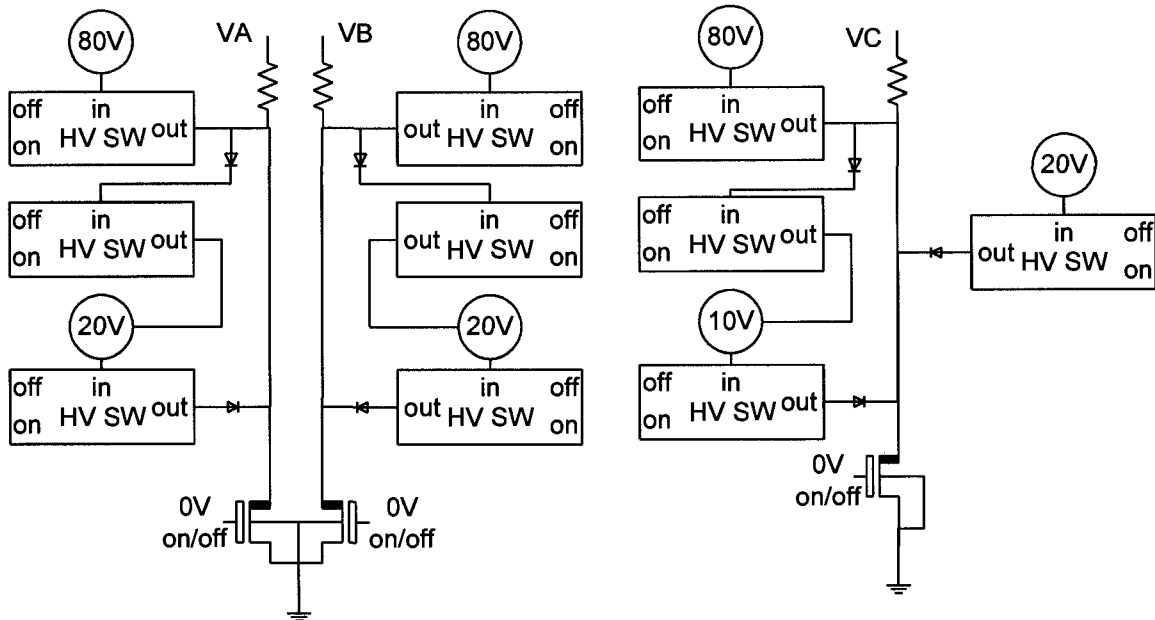


Figure 4.1.2 - HV Switching Block Diagram

4.2 Level Shifter Design

The DMOS transistors, while having the ability to work with large source to drain voltages, do not have the same ability to support these voltages from gate to source. The key to operating a high voltage transistor efficiently is then the ability to shift control signals from a ground state to a high voltage state in order to operate the gates of the PDMOS transistors. A basic active static level shifter can be constructed with a common source amplifier and inverter. This is shown in Figure 4.2.1 with the level shifter connected to a HV inverter stage.

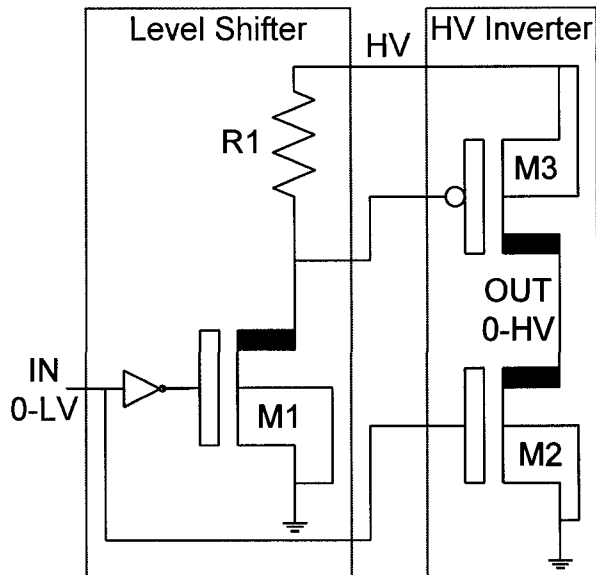


Figure 4.2.1 - Basic Active Static Level Shifter

The analysis of the operation of this level shifter is quite straightforward. The resistance $R1$ is simply picked and ratioed to the on resistance of $M1$ so that, when $M1$ is turned on, the voltage drop across $R1$ will turn on $M3$. Since there is an inverter between the input and $M1$, $M2$ will operate in the inverse and be off when $M3$ is on. A simple pictorial representation of the voltages involved is shown in Figure 4.2.2. The major disadvantage of this design is the constant current required through the level shifter when $M3$ is to be held on. For high speed operation $R1$ must be small enough to allow the gate capacitance of $M3$ to be switched quickly. The smaller the value of $R1$, the larger the current and power used by the level shifter to create the necessary voltage swing needed at the gate of $M3$. The level shifter could easily be modified with $R1$ replaced by a low voltage PMOS transistor in a floating well that is configured to exploit its resistance in a diode configuration with the gate tied to the drain.

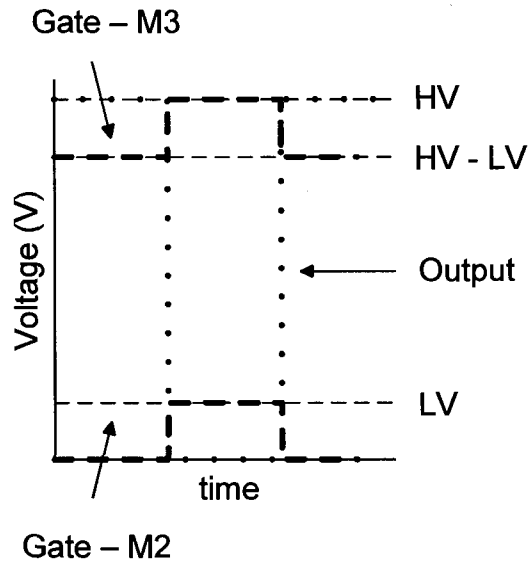


Figure 4.2.2 - Basic Active Static Level Shifter Voltages

This common design has been modified many times. The most prevalent modification involves putting a matched pair of the basic level shifters together in a differential configuration with a PMOS transistor used as the load resistance. The PMOS gates are cross-coupled so that when one side is turned on, the other is off, but still holds the gate of the PMOS on. A complete discussion of many of these modifications as well as high voltage op-amp design can be found in [12] with other examples in [14, 15]. Unfortunately, most of these designs involve using high voltage transistors to handle the voltages in the level shifter. There are many issues when using very high voltages (80 V) since the gates of the DMOS transistors can not handle the same voltage that occurs at the drain. When modified for these high voltages these level shifters have poor performance and large power losses. A solution to this problem was proposed in [15] where biased MOS transistors were stacked up drain to source to support the high voltages, with each gate biased at a successively higher voltage. This solution,

however, becomes cumbersome for very high voltages (80 V) because it requires a stack of 16 transistors and the generation of all the appropriate bias voltages. It also could have limitations when imposing the constraint of varying the HV applied at the top of the stack.

If the level shifter could be shut off while keeping the PDMOS gate on, a majority of power consumption could be eliminated. A novel solution to this effect was proposed in [16]. The proposed level-shifted high voltage switch schematic is shown in Figure 4.2.3. Here three active level shifters are combined in a configuration with low voltage logic to allow the gate of the PDMOS output transistor to be opened or closed by activating the appropriate pull-up or pull-down shifter and then strobing it on or off. In between the strobing operations the gate of the PDMOS output transistor is disconnected and allowed to float in either an on or off state. It is thus an actively driven dynamic level shifter, with PDMOS gate acting like the capacitive node in a dynamic logic circuit.

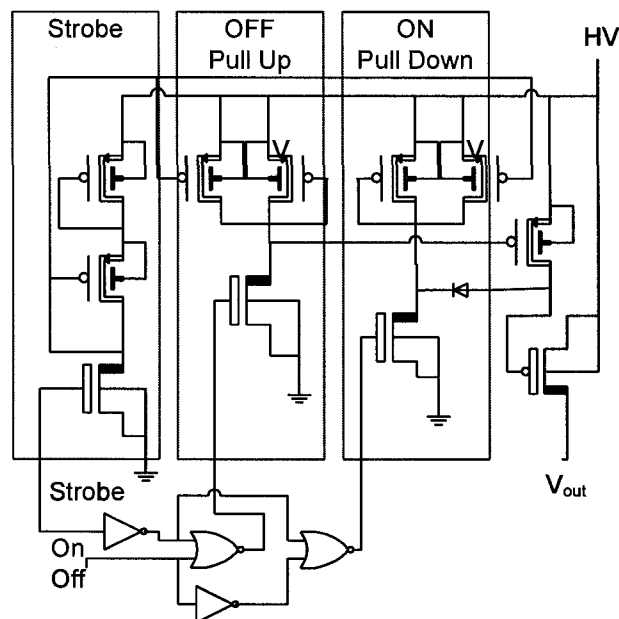


Figure 4.2.3 – Active Dynamic Level Shifted Switch

For the actual design of the high voltage switches in the RF MEMS switch driver circuit, the basic idea of the floating PDMOS gate was kept and a new passive capacitively coupled level shifting mechanism was added to remove the pulses of current occurring during the strobe phase in the previous design. A schematic of the high voltage switch used in the final design is shown in Figure 4.2.4. Here low voltage drivers (TTL) are coupled to the gates of the high voltage PDMOS M1 and the floating low voltage PMOS M2.

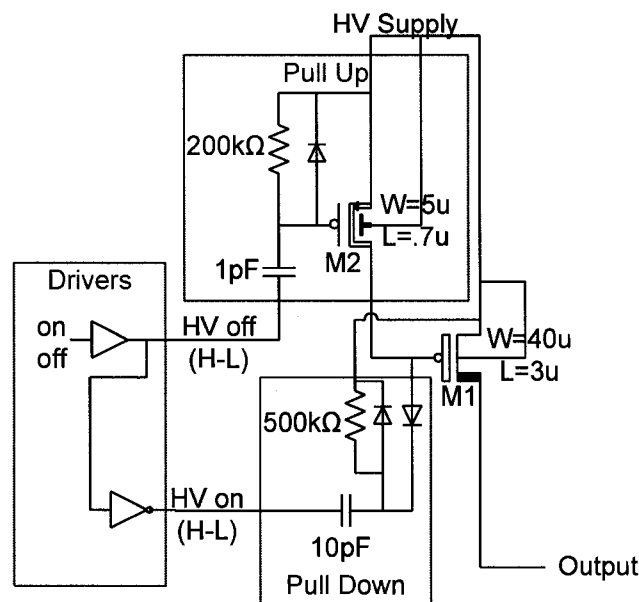


Figure 4.2.4 - Passive Dynamic Level Shifted Switch

The analysis of its operation is as follows. When a low to high transition takes place at the on-off input, the HV on signal follows and pulls the bottom electrode of the 10 pF cap from 5 V to 0 V. This causes the potential of the top electrode to drop a similar amount. The top electrode is connected through a diode to the gate of the M1 which has a capacitance. The result is capacitive voltage division at the gate of M1. If the 10 pF cap is much larger than the gate capacitance of the PDMOS transistor, the gate will be pulled lower and M1 will

turn on. Since there initially needs to be a voltage to charge up the top plate of the 10 pF capacitor, a large 500 k Ω resistor was added from it to the HV supply, thereby charging it back to the supply voltage. The diode connection to the gate now becomes reversed biased and thus the gate voltage does not follow higher and floats in the on state.

To turn off M1, a second shifter was added to control the gate of a small floating PMOS M2. As the transition at the on-off input goes from high to low, the bottom electrode of the 1 pF cap is pulled lower, thus pulling the gate of M2 down via the same mechanism as explained above. The gate of M2 again has a large 200 k Ω resistor tied to it to provide a reference voltage. Since there is no diode between the cap and gate, M2 will only turn on momentarily, but this is enough to charge the gate of M1 back up and turn it off. M1 is disconnected again after the small PMOS transistor turns off. Diodes from the top plates of both capacitors to the HV supply prevent the voltages from being pushed above the supply when resetting the bottom plate potential to 5 V. Simulation results of the operation of the level shifter are included in Section 5.2.

There are risks and tradeoffs associated with each of these designs. Simulations of the power consumption for all three designs were done in the AMI I2T100 technology and layout area was estimated for each; the results are shown in Figure 4.2.5. The dynamic level shifter shows a five to six order of magnitude improvement in power consumption over the static level shifter at a cost of approximately double the circuit area. When modified for the passive design, a further two orders of magnitude were reduced from power consumption

with a three fold increase in area. Most of the area consumption is due to the nature of the capacitors used. The only capacitors available above 30 V differential between plates are passive poly-metal-metal stacks with low capacitance per area. However Figure 4.2.5 also shows the comparison (square box) with a MV (less than 30 V) level-shifted switch where a poly-poly capacitor can be used with a much higher capacitance per unit area. As a comparison, the power consumption and area of a minimum sized inverter and the RF MEMS switch are also provided.

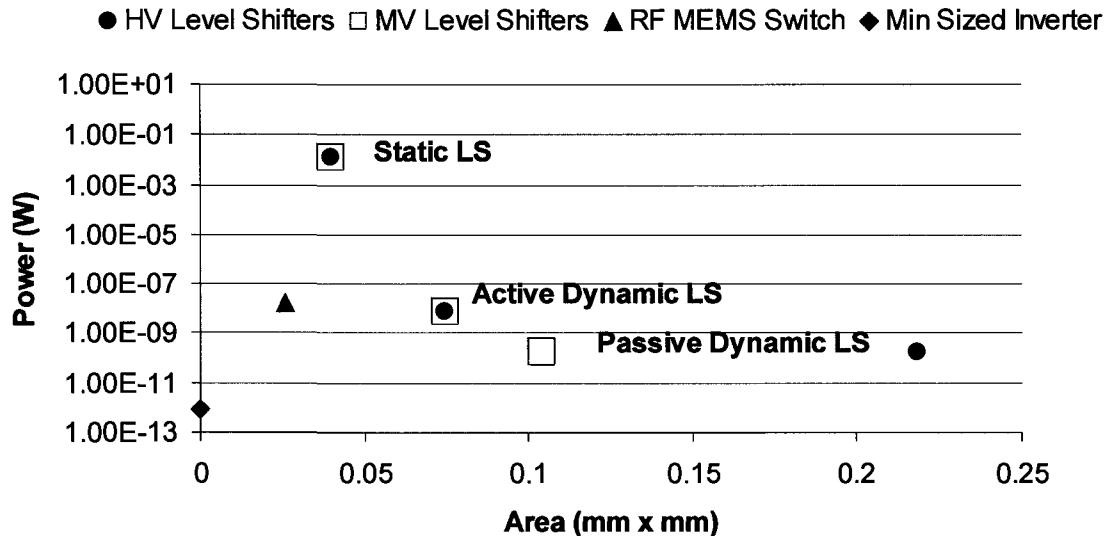


Figure 4.2.5 - Level Shifter Comparison of Area and Power Consumption

4.3 Waveform Generator Control Design

Several different approaches were studied for the control portion of the system. The most straightforward would be a sequential method where a high frequency clock is divided down in something like a state machine. A simplified diagram of this approach is shown in Figure 4.3.1. The sequential machine

outputs would then drive the combinational logic necessary to generate the proper signals to drive the DMOS switches via the level shifters. To obtain the required minimum resolution of 1 μ s the clock and first flip flop must run at 1 MHz. Each successive flip-flop would run at half the previous flops rate if a ripple counter method were used. A D-Flop in the AMI I2T1000 technology is rated at 11.65 μ W/MHz, thus giving a power just over 23 μ W for all the flops in the state machine. If compared to the values in Figure 4.2.5, this looks rather power hungry considering the MEMS switch could consume up to two orders of magnitude less.

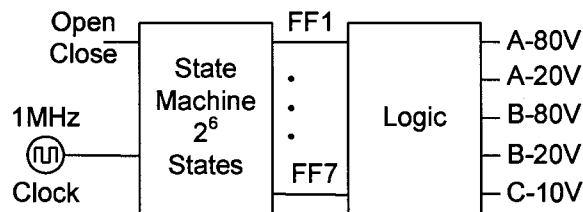


Figure 4.3.1 - Sequential Control

Since power consumption is directly related to the clock frequency, a design with a clock that runs only at the lowest frequency (the period of the hold down waveform, 10-100Hz) would greatly reduce the power. The pull-down waveform is a known sequence of a HV kick followed by a lower voltage kick and then a hold voltage of the same polarity. By creating varying length pulses driven from the incoming rising edge of the open/close signal, and then allowing the hold-down waveform to follow the clock, the desired waveform can be created. This approach was used in the actual design shown in Figure 4.3.2 where only 2 flops were used, both of which only change states with the frequency of the open/close signal (MEMS switch operation) or the clock.

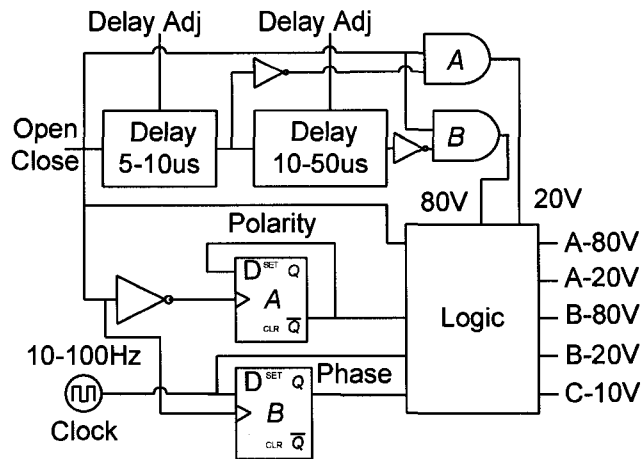


Figure 4.3.2 - Combinational Logic Control

The incoming edge of the open/close signal creates two pulses. Each delay is adjustable via several bit lines that allow more capacitance to be switched into an RC delay. Each delay corresponds to the time period needed in each stage of the pull-down portion of the waveform shown in Figure 3.1.1. By using an AND (or NAND) gate between the input and output, a pulse will be created corresponding roughly to the delay. These pulses are then fed into a logical block along with the original open/close signal to allow triggering of the pull-down signal. The hold-down signal is a function of the clock applied. The phase of the clock when the open/close signal is applied is stored in flop B and the logic will flip the phase of the clock if open/close is applied when the clock is low, thus keeping the polarity of the hold-down waveform correct. Since the polarity of the entire bias waveform flips during every other activation, as shown previously in Figure 3.1.2, the previous state is held in flop A and used in the logic block to invert the terminal A and B operation signals.

4.4 Interface Logic and Drivers Design

Each level shifter needs a signal from the TTL logic with rapid edge transitions to work properly. The waveform generator also generates only signals corresponding to the appropriate voltage levels to be applied. Thus there needs to be a second level of glue-logic and inverter scaling that ensures proper operation of the HV system. The schematic representations of this logic are shown in Figure 4.4.1 and Figure 4.4.2. The A or B terminal operation is relatively straightforward. If there is no high voltage to be applied, the terminal should be grounded; the OR gate accomplishes this task. The inverters are scaled up in order to facilitate driving the level shifters to which they are attached. The pull-up and pull-down functions for each PDMOS gate are inversed by adding a third inverter to the pull down output.

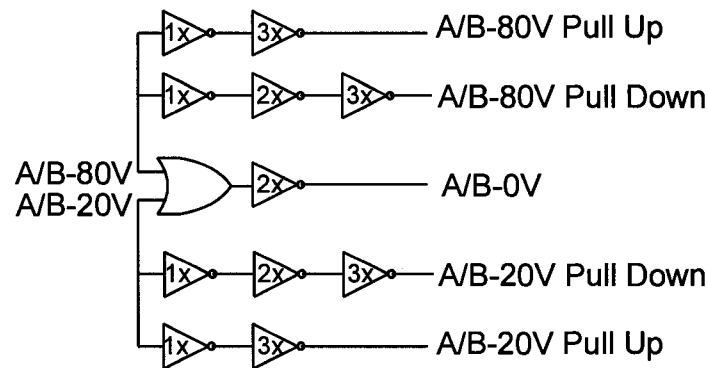


Figure 4.4.1 - A and B Terminal Interface Logic and Drivers

The logic for the C terminal is a little more complicated due to the asymmetric operation. Terminal A changes its pull-down behavior due to the alternating polarity of the waveform during each successive activation. Terminal C should only be 80 V when terminal A is 80 V thus the two inverters are added to drive C-80V from the A-80 signal. Terminal C should only be 20 V if Terminal

A is 20 V and Terminal B is 80 V during the pull-down of reversed polarity. This outcome is produced by the AND gate driving the C-20V Pull-Up and Pull-Down drivers. Terminal C should only be grounded when there is no HV (C-20V, C-10V, A-80V) applied and this outcome is produced by the three terminal NOR gate and associated driver. Another special case for Terminal C requires that a 10 V differential from terminal B to C be maintained when terminal B swings from 20 V to 0 V. Thus terminal C must be a constant 10 V. To maintain this level with the dynamic level shifter over long periods (100's of milliseconds), the gate must be periodically refreshed, so that it stays on. C-10 Pull-Up must then be periodically pulsed. This is accomplished with a delay and an XOR gate attached to the C-10V and A-20V signals. Therefore, C-10V Pull-Up is pulsed and activated at the beginning of the hold-down cycle and on the rising edge of the clock during the hold-down cycle.

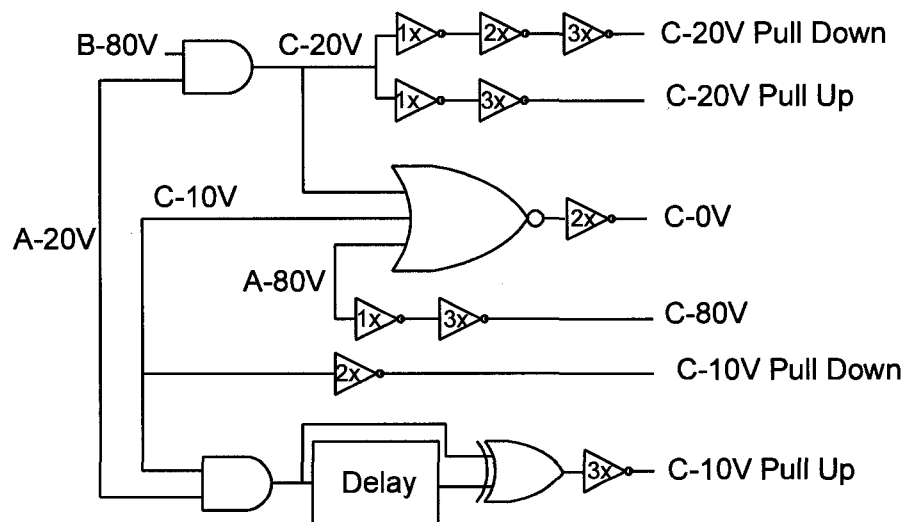


Figure 4.4.2 - C Terminal Interface Logic and Drivers

CHAPTER 5

LAYOUT, SIMULATION, AND TESTING

This chapter shows the simulation, layout and testing results for the design. The first section describes the layout and the implications of high voltage for the layout process. Section 5.2 shows simulations of the high voltage level shifter as well as results for the complete design. Section 5.3 describes the testing process and results of the prototype.

5.1 Layout

The layout of the high voltage PDMOS switch with its associated level shifter, shown schematically in Figure 4.2.4, is shown in Figure 5.1.1. The medium voltage (less than 30 V) version, which differs only in the capacitor implementation, is shown in Figure 5.1.2. The relatively large size of the HV capacitors can be seen in comparison to the MV capacitors and to the PDMOS itself. The large square on the left is the 10 pF capacitor, and the smaller square on the top is the 1 pF capacitor. The pull up and pull down sections are labeled as well.

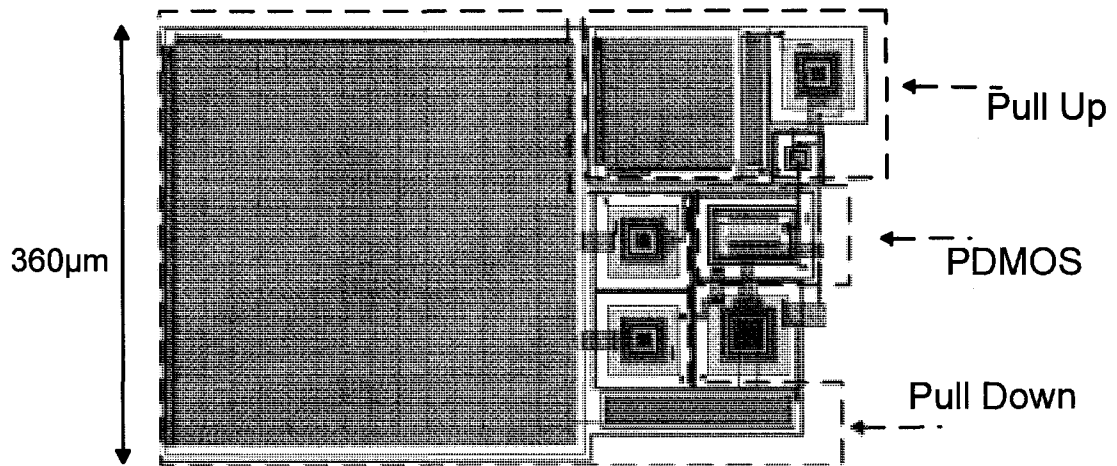


Figure 5.1.1 – HV Level Shifted PDMOS Layout

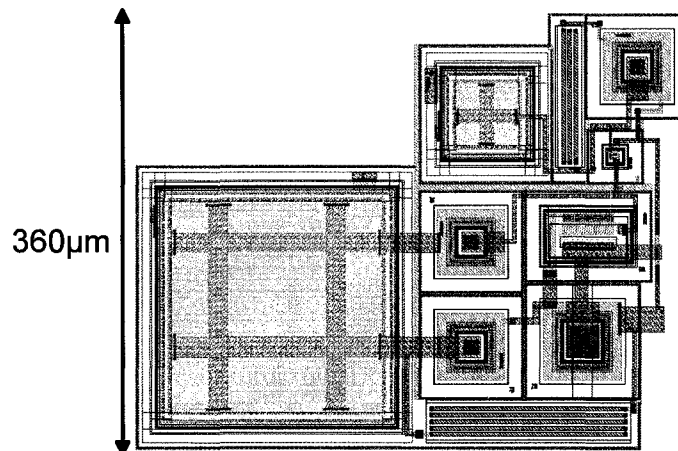


Figure 5.1.2 - MV Level Shifted PDMOS Layout

The low voltage waveform generator is shown in Figure 5.1.3. The RC delays are clearly evident. The flip flops and logic used were all standard library cells provided in the AMI I2T100 design kit. All the logic was grouped together, while the related logic and drivers for the delays were kept closer to the actual resistors and capacitors to minimize parasitic effects on the performance. The same methodology was used during the layout of the interface logic and level shifter drivers shown in Figure 5.1.4. Here the delay for the strobe is shown along

with its own logic and drivers separated from the general logic as well as drivers used to control the other level shifters.

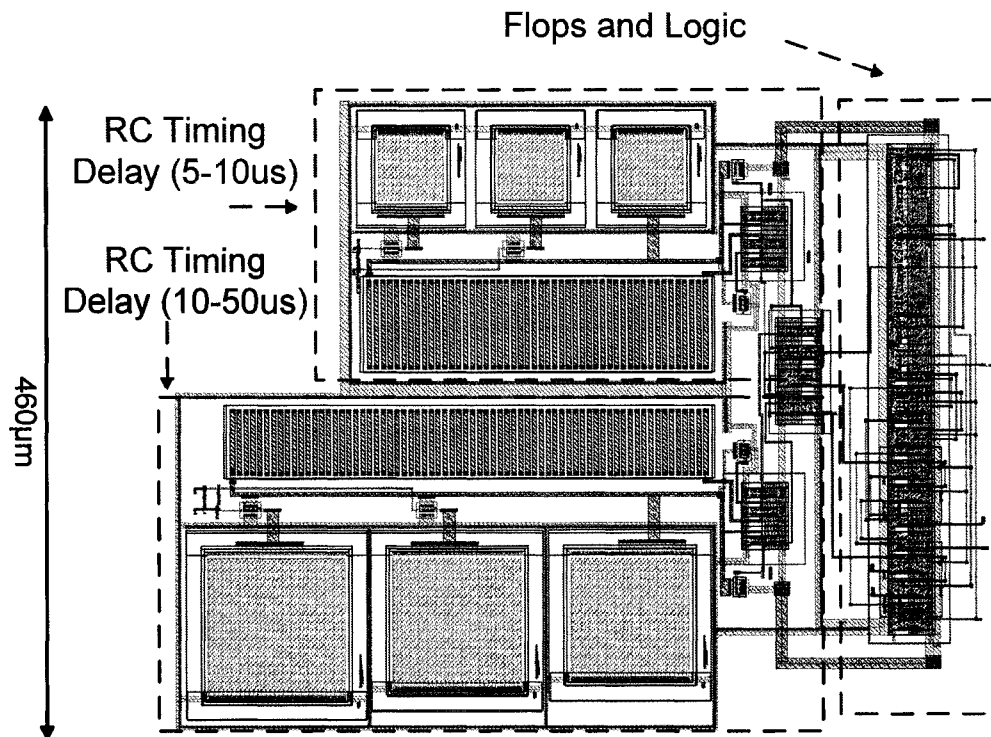


Figure 5.1.3 - Waveform Generator Layout

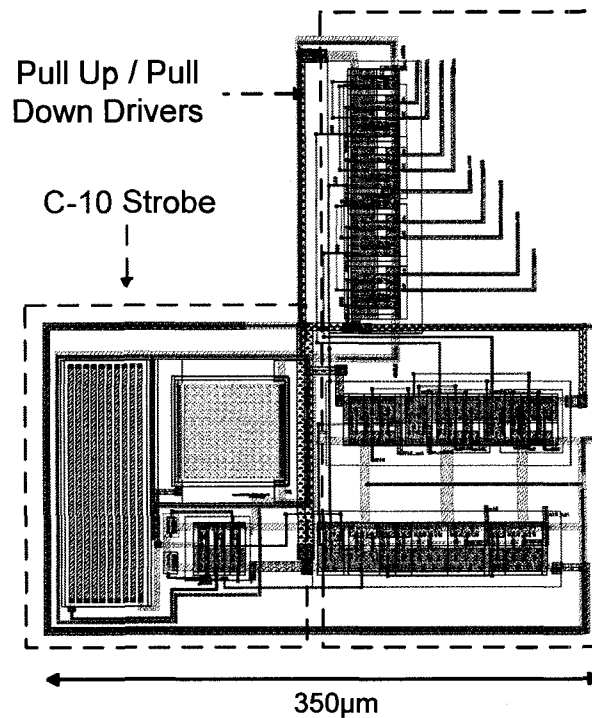


Figure 5.1.4 - Interface Logic and Drivers Layout

A general consideration when mixing standard CMOS logic and high voltage logic is that they should be placed so that the metal connections do not overlap. Metal lines with high voltage transients should never cross low voltage lines since coupling may induce transients on the low voltage line above the threshold for the technology. In order to protect against fluctuations in the substrate, many contacts to ground should be included around and throughout these sections. Keeping the substrate stable also helps keep any unwanted parasitic bipolar transistors that occur naturally in the DMOS transistor layouts from being activated. A specific discussion of these topics for the I2T100 technology is included in [3].

A complete top-down view of the design is shown in Figure 5.1.5. The high and low voltage sections are kept separate. Standard Input-Output (IO) cells

were used for all low voltage interfacing. In blank areas of the pad ring, decoupling capacitors were added on the V_{dd} rail. All low voltage IO's include Electro Static Discharge (ESD) protection. The high voltage structures, on the other hand, do not include any ESD and are in fact just metal pads. The high and low voltage level shifters and switches for the A and B terminals are located in the middle of the chip, and are mirrored one on top of the other. The terminal C switches are on the right hand side. The interface logic and drivers are at the bottom left corner, and all connections to the level shifters trace around the high voltage section to the appropriate switch before entering the high voltage section. The waveform generator is above the interface logic. Total area is approximately 9 mm^2 .

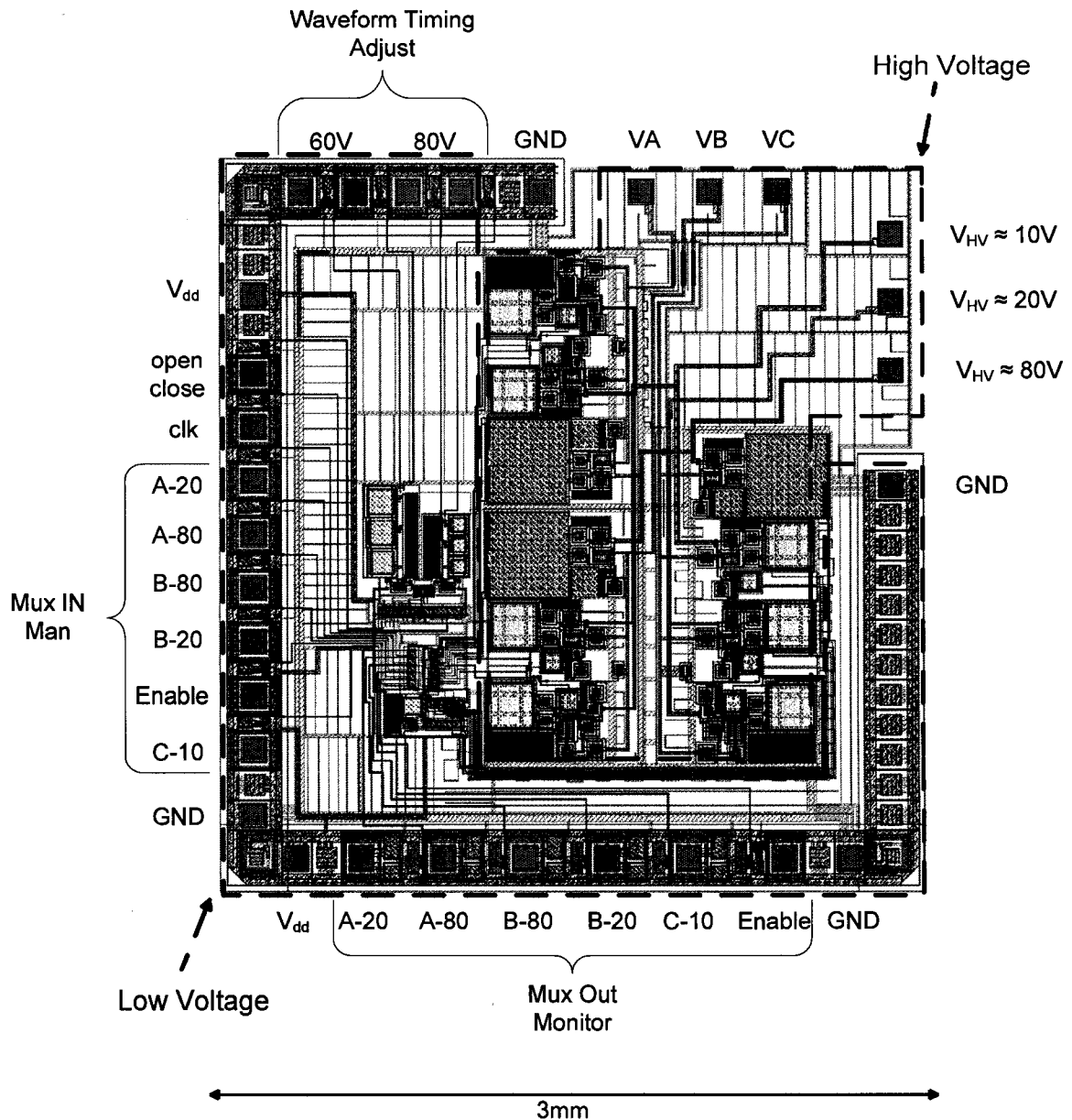


Figure 5.1.5 - Top Level Layout

5.2 Simulation

All aspects of the design were simulated in SPICE extensively. A simulation of the level-shifted high voltage PMOS switch is presented in Figure 5.2.1. The simulation shows the inverter connected to the pull-down circuit, shown previously in Figure 4.2.4, drops the low voltage electrode of the pull-down

capacitor from 5 V to 0 V as shown in the second graph down. The high voltage electrode of the capacitor drops as well from 80 V to approximately 75 V as does the gate of the PDMOS transistor (minus a diode drop). As the resistor charges up the high voltage electrode of the cap, the diode becomes reverse biased letting the PDMOS gate remain at approximately 75.5 V. The PDMOS is then 'on' and the drain voltage rises to 80 V.

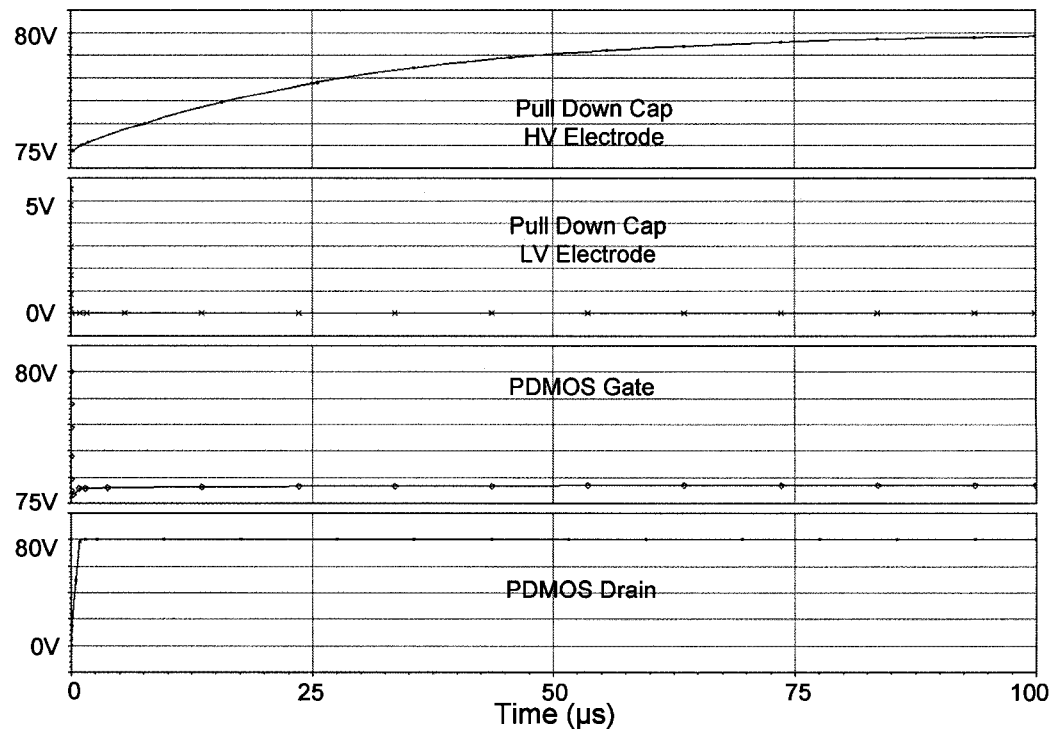


Figure 5.2.1 - Level Shifted HV PMOS Gate Pull-Down Simulation

A simulation of the PDMOS turning off is shown in Figure 5.2.2. As the low voltage electrode of the 1 pF capacitor is pulled from 5 V to 0 V, the small floating PMOS transistor's gate is momentarily pulled down and it momentarily turns on. A low resistance connection is then made between the high voltage source and the gate of the PDMOS transistor, thus rapidly charging it to 80 V and turning the PDMOS off. The drain voltage falls rapidly to 0 V. These simulations show the

theoretical performance of this design based on SPICE simulations without accounting for parasitic capacitances or other shortcomings in the device models. Faults were found in the design during testing that shows the operation of this circuit does not follow these ideal simulations. A thorough discussion of this disparity is included later in Section 5.3.

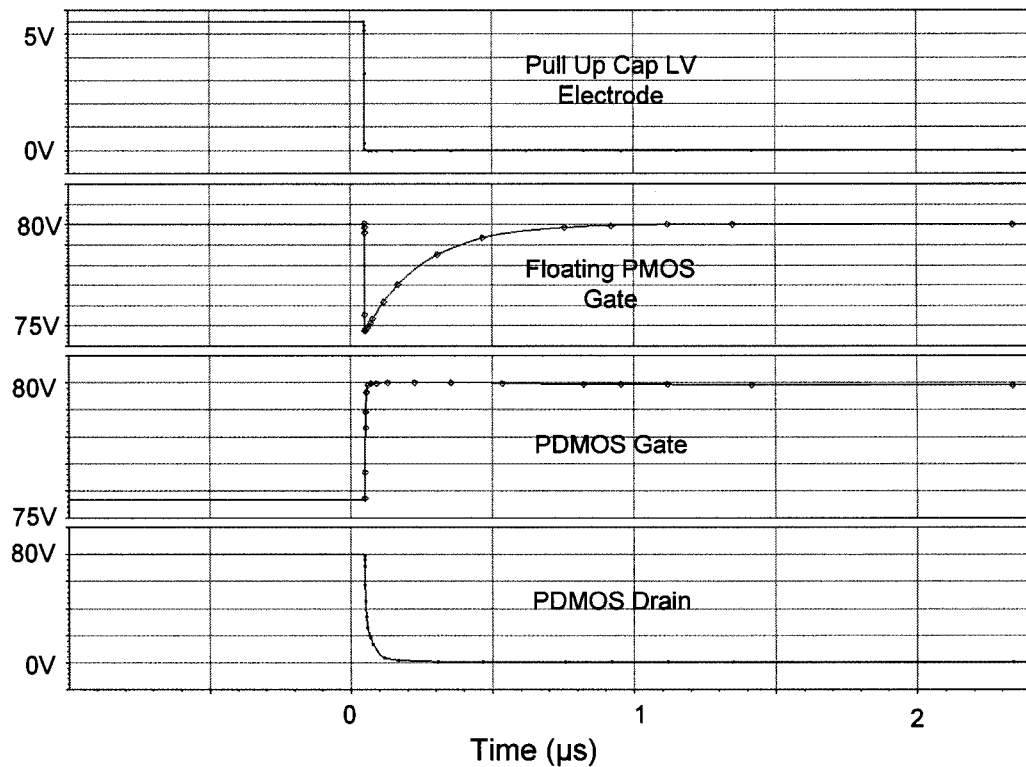


Figure 5.2.2 - Level Shifted HV PMOS Gate Pull-Up Simulation

A complete simulation of the entire MEMS switch driver, as sent to manufacturing, was run using the worst case capacitance model of the RF MEMS switch shown previously in Figure 2.1.3. The results are shown in Figure 5.2.3. Here the clock is applied with the open/close signal; all other timing, manual, and test inputs and outputs were held constant or disabled. The differential output of the three driver terminals is shown twice. The first view is

over an extended time frame, which shows the correct operation of these signals and the polarity reversal of the driver waveform. The second is a magnified view of the HV pull-down portion of the waveform, which shows the correct voltage levels and operation.

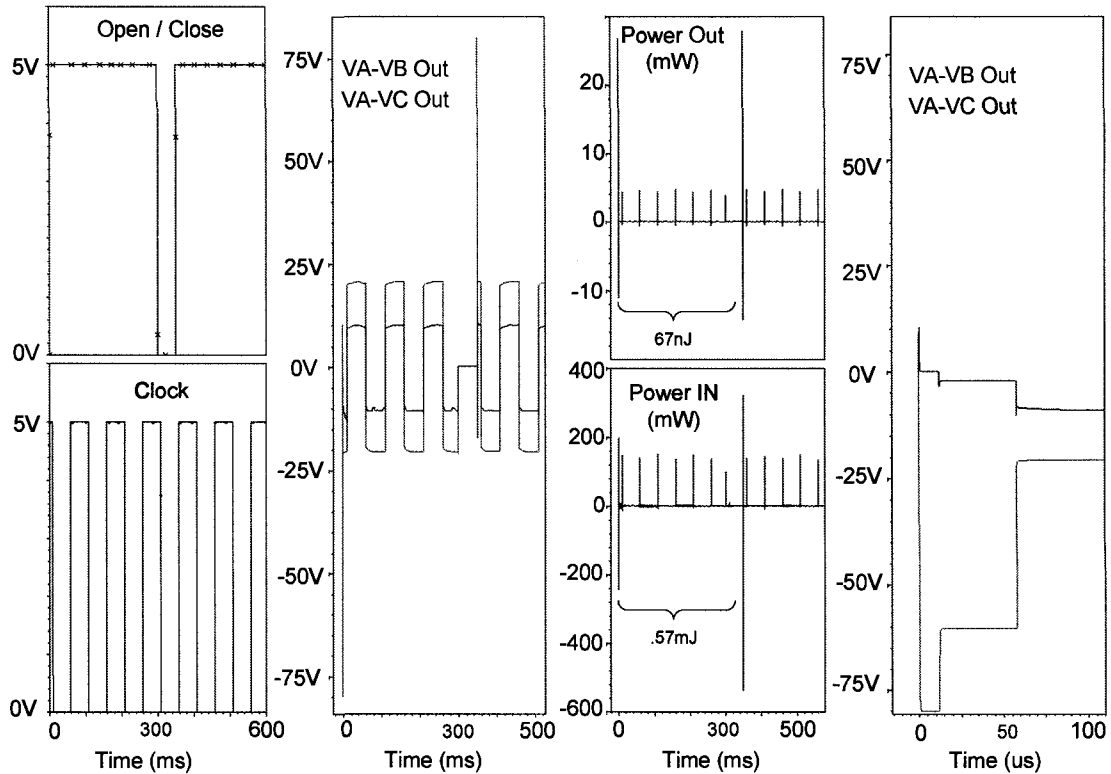


Figure 5.2.3 - Operational Simulation of RF MEMS Switch Driver

The instantaneous power output of all three output terminals was summed together and a numerical integration was performed to arrive at an energy output calculation. The same was done for all voltage sources entering the chip. From these two quantities the efficiency of the chip was calculated and found to be 0.01 %. This would seem a rather poor result but, as mentioned in Section 3.1, it could be expected due to the technology and very low power levels. If the RF MEMS switch is assumed to be closed only once per second, an average power

level of 1.7 mW can be estimated from the simulation. This result compares favorably to the commercial examples given in Table 3.1.1.

5.3 Testing

Since the chips were manufactured as part of a multi-project run, testing the wafer or individual die unpackaged was not an option. The chips were packaged in a standard 40 pin Dual In-Line Package (DIP) as shown in Figure 5.3.1. The high voltage output terminals were bonded to the package pins with the lowest parasitic capacitance and inductance to facilitate more accurate testing. After the chip was packaged, the IC was placed in a test bed that was constructed with four bench top variable DC power supplies, National Instruments LabVIEW software and hardware interfaces, and a multi-channel oscilloscope. A diagram of the test bed is shown in Figure 5.3.2. A standard breadboard was used to facilitate the interconnections.

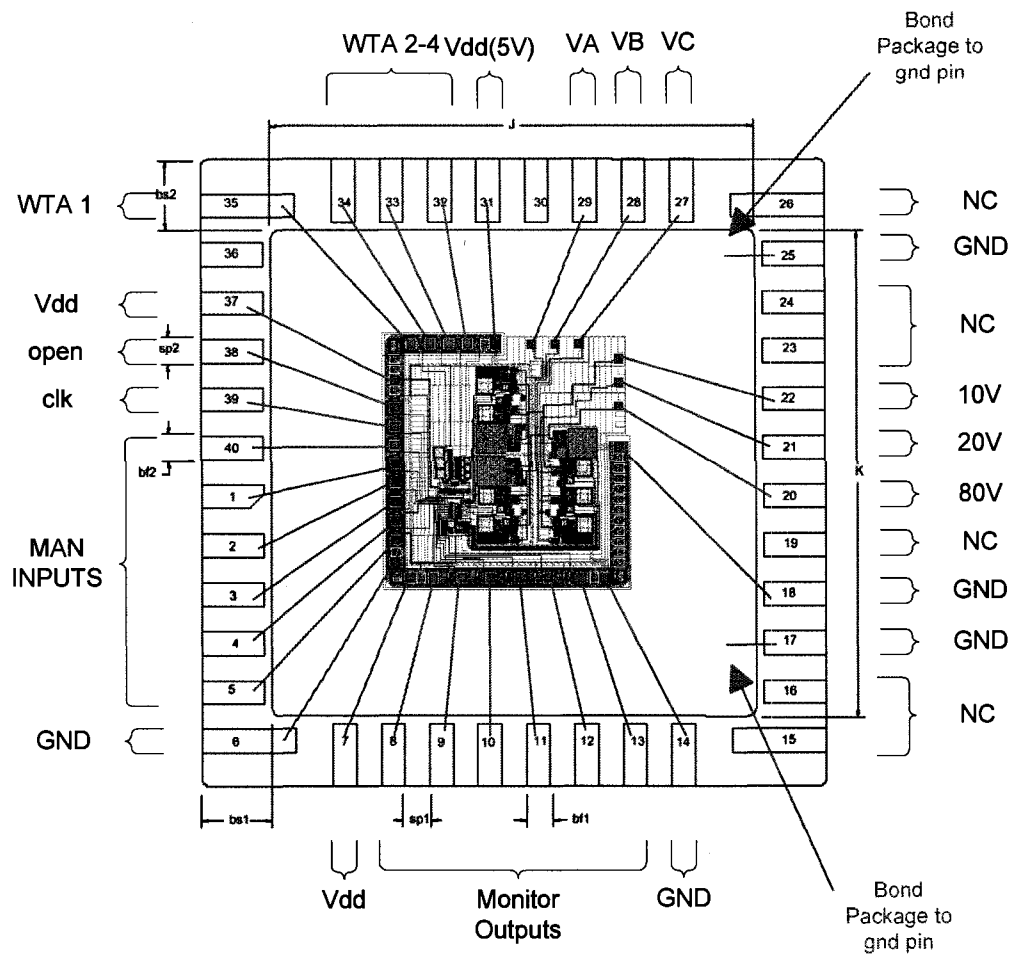


Figure 5.3.1 - Package Bonding Diagram

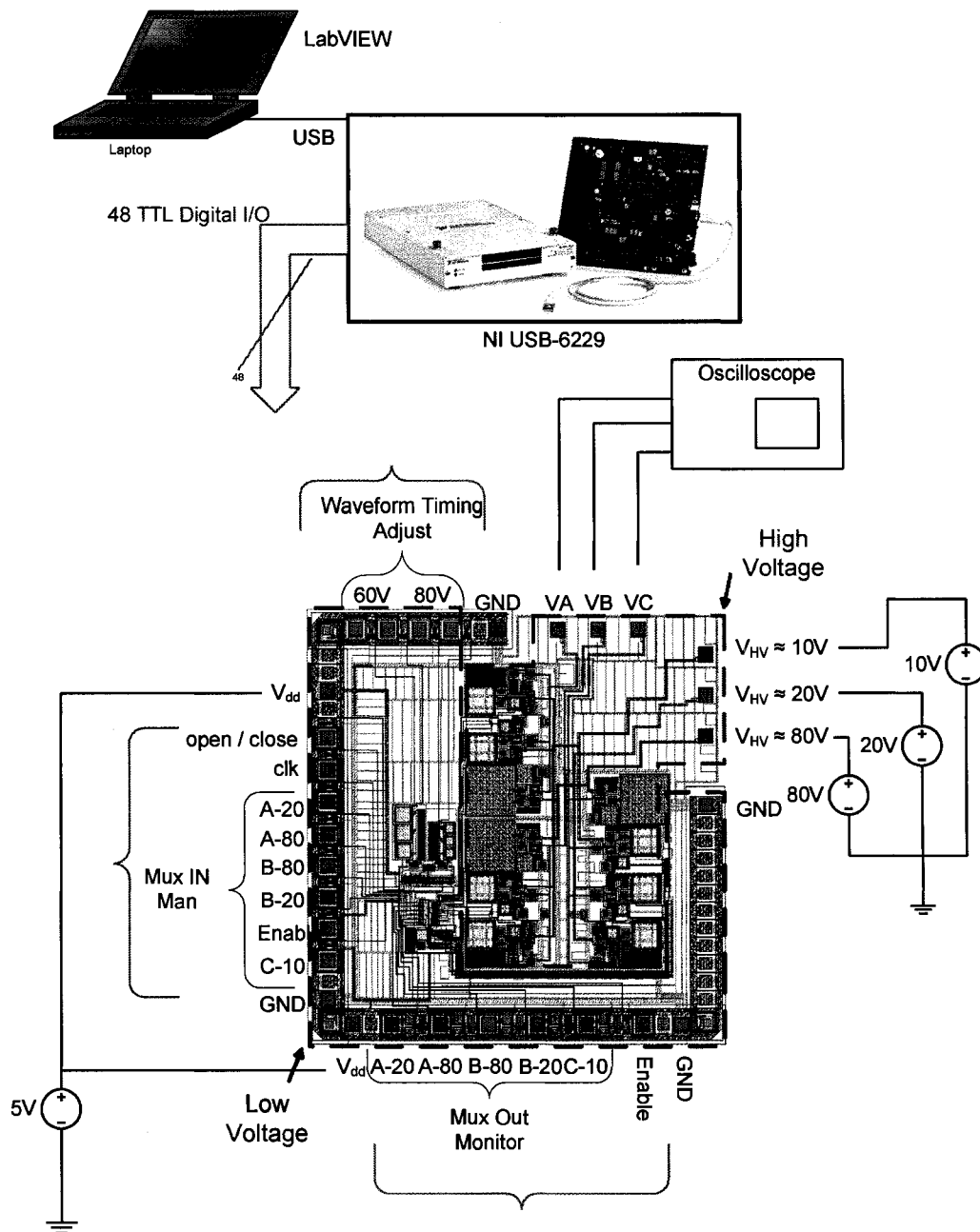


Figure 5.3.2 - Test Bench Diagram

Testing began with only the low voltage systems. An open/close signal and clock were created. The manual mux outputs were hardwired 'on' and the resulting outputs were captured on the LabVIEW Software and analyzed for correct operation. After this was accomplished, the high voltage systems were powered up by slowly increasing each voltage source to its proper voltage using

the variable control on each supply. The sequence of power-up was done going from the lowest voltage supply to the highest voltage supply, and each supply was current limited as low as possible. After confirming that there were no shorts the clock and open/close signal were again applied and the resultant high voltage waveforms were measured on the oscilloscope.

The automated high voltage output that was observed was only partially correct. A positive polarity waveform is shown in Figure 5.3.3. The left hand screen shot shows the full bias waveform output swinging from +20 V to -20V differentially from terminal A to terminal B. The high voltage (80 V) kick at the very beginning does not reach its full potential, as can be seen in the magnified in screen shot on the right. The terminal C voltage is also missing some of the kick voltage it should have to follow terminal A; both should reach 80V. Other aspects of the waveform appeared as designed. The kick waveform did change polarity automatically and the timing was also variable via the four timing inputs. The supply for V_{dd} was varied to see the effect on the resulting waveform. Rise times for the kick improved but peak voltage was still well short of its target value.

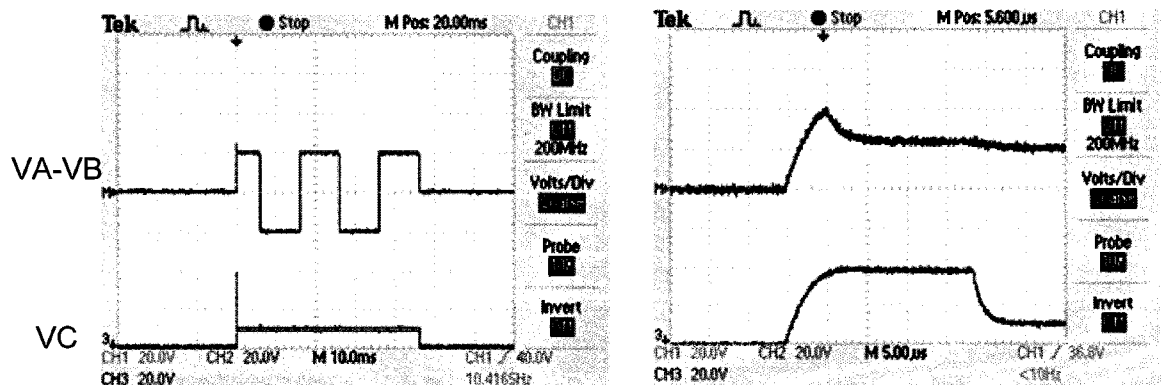


Figure 5.3.3 - Internally Generated Output Waveform (Full and Magnified)

The first consideration for this discrepancy was that the oscilloscope was loading down the outputs. The scope probes are rated at 16 pF, or five times higher than the designed for load. Since 50 k Ω resistors were included on the outputs, the extra testing load affects the rise and fall times observed by the scope. To investigate further, the manual inputs of the circuit were used to make longer 80 V pulses on terminal A and then terminal B. Surprisingly, in Figure 5.3.4 it is clear that the pulse comes very close to its maximum when actuated individually. V_{dd} was again varied up to 6 V and down to 4 V to see the effect. Comparing the 5 V case in Figure 5.3.4 to the 6 V and 4 V cases in Figure 5.3.5, it is clear that the PDMOS does not get turned on fully. This result can be accounted for in a SPICE simulation if the drain to source capacitance of the PDMOS transistor is not properly modeled. Thus, the result is a feedback capacitance that, as the drain voltage swings from 0-80 V pushes the gate voltage from a nominal 76 V to 79 V (PDMOS threshold is $|V_{th}|=1$ V), thus turning the transistor off before the end of the rise time.

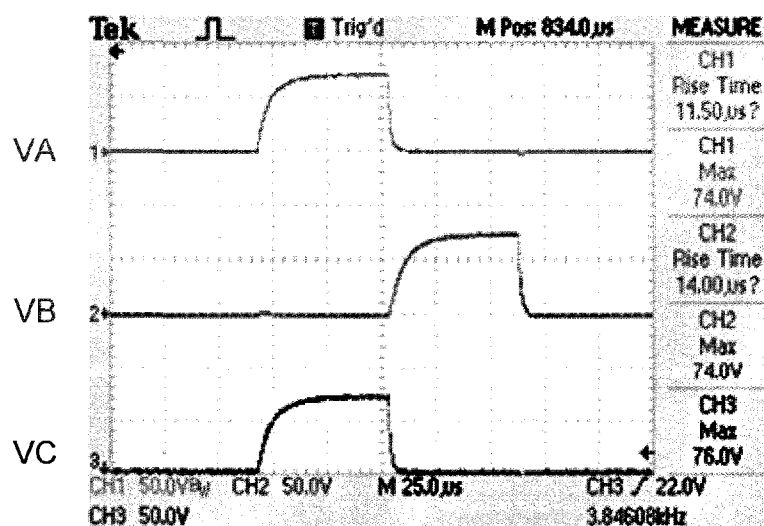


Figure 5.3.4 - Manually Generated 80V Pulses at $V_{dd}=5$ V

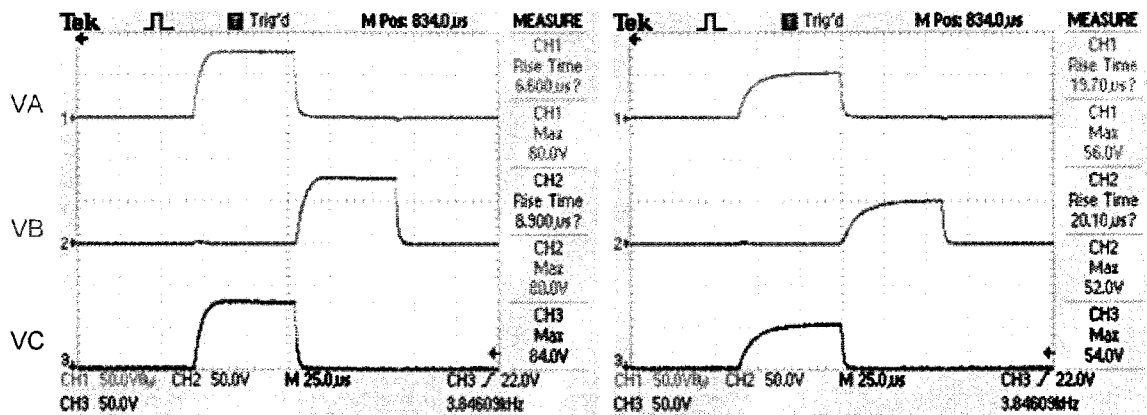


Figure 5.3.5 - Manually Generated 80V Pulses at $V_{dd}=6$ V and $V_{dd}=4$ V

Another experiment was run with pulses of 80 V and 20 V in sequence.

From Figure 5.3.6 it is evident that just using the 20 V PDMOS transistor decreases the voltage output of the 80 V PDMOS. This can also be explained in simulation with the addition of a drain-to-gate capacitance on the NDMOS transistors that allows charge from a higher voltage source to drain into a lower voltage supply as shown in Figure 4.1.2. The result is similar to the PDMOS behavior, except that as the drain increases from 0 V to 80 V, the gate of the transistor is turned on by going from a nominal 20 V to something over 22 V (NDMOS threshold is $|V_{th}|=2.2$ V).

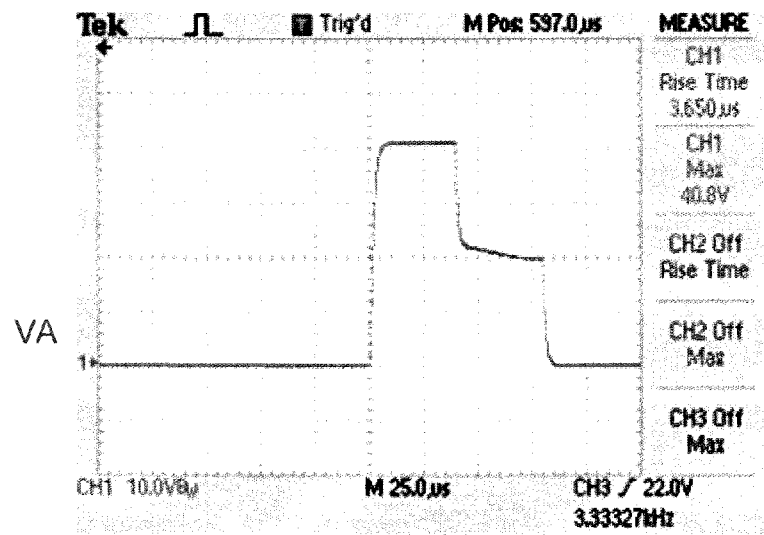


Figure 5.3.6 - Manually Generated 80V - 20V Pulse

CHAPTER 6

MODIFICATIONS, FUTURE WORK, AND CONCLUSIONS

6.1 Design Modifications

The results of testing presented in 5.3 suggest a fault in the process model that was used to design the circuit. The SPICE model is constructed in a piecewise manner and is a combination of several standard BSIM3 low voltage transistors plus a resistor and diodes representing the increased drain resistance due to the lengthened drain and parasitics to the substrate. Results reported in [12] of drain-to-gate capacitance of a similar technology show that extra capacitance in the 100 fF range is entirely possible.

The design can be modified to deal with these problems. The easiest fix would be to modify the resistor and capacitor values that couple the DMOS gates in the level shifters. A longer RC time would allow the gate to be activated longer. Extra capacitance could be added to the gate node itself so that the gate-to-drain capacitance would have a less dominant effect than that due to the level shifter. The second modification could be done in the digital control circuitry. Since the NDMOS transistors are forced on and form a current leak, they could be turned off when other events (80 V transitions) are occurring. This could be accomplished by modifications in the interface and driver logic. A complete

change in the interface logic might allow all DMOS transistors to be reset to the appropriate gate condition when any change occurs in any one of the other DMOS states. This can be accomplished since there is individual access to the pull-up and pull-down terminals of each DMOS gate. Thus, a PDMOS that is off can be turned off again without ever turning it on and vice-versa for an NDMOS.

6.2 Future Work

The bias generator presented here is only applicable to a single RF MEMS switch. A multi-switch version could be constructed to control more advanced functions of the RF MEMS switch technology. This could include an integrated system to control multi-pole, multi-throw switches as well as series-shunt switches. These configurations would have wide uses as a total system. Integrated DC-DC conversion could also be added to allow the system to eliminate some of the many power supplies needed for operation. Some research time was spent on these possibilities and an overview of the options available is presented in 0. An internally generated clock would also be of use by eliminating one of the two inputs needed currently.

6.3 Conclusions

An integrated solution to the control of the actuation of a RF MEMS switch was presented. A novel passive dynamic level shifter was designed and fabricated that allows the gate of a PDMOS transistor floating at high voltage to be coupled capacitively to the standard low voltage logic. It maintains its state dynamically using the built in capacitance of the PDMOS transistor itself. A novel

digital control circuit was also designed, and fabricated, that allows the proper sequence of signals to be generated by delaying the actuation signal and combining it with a low frequency clock through a series of digital logic gates. The control circuit uses only two flip-flops to maintain the current phase of the clock and the high voltage waveform.

The bias driver provides switching times of 1 μs , between voltage sources, and has low power consumption of several mW that could allow a MEMS switch system to compare favorably to existing non-MEMS solutions. The level shifters in the driver provide the ability to vary the high voltage sources, while the waveform controller provides the ability to vary the timing of the waveform. This flexibility makes the bias driver useful for future applications and varying switch designs with variable biasing constraints.

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APPENDICES

APPENDIX A

CALCULATIONS

RF MEMS Micro switch Ideal Bias Power Consumption

Using the model shown in Figure 2.1.3 and the waveform shown in Figure 3.1.1, the power can be calculated in a piecewise fashion with the commonly found equation for the energy stored in a capacitor, shown in Equation 1. Several different stored energies are calculated in Equation 2. To calculate the waveform, a worst-case scenario will be assumed for the 60V level in the pull-down, such that terminal A is charged to 80 V and then terminal B is charged to 20 V. Also, only the positive waveform of Figure 2.1.1 will be considered and thus terminal C will follow terminal A to 80 V. It is then relatively easy to add the energy for all of the positive going transitions as shown in Equation 3 and Equation 4. It should be obvious that a faster cycle time of the RF MEMS switch, and thus less flipping of the hold-down voltages, allows the pull-down energy to dominate, while a longer switch cycle allows the hold-down energy sum to dominate. If each capacitor energy is normalized to 1 second it can be expressed in terms of power (Watts). The vales can then be calculated in terms of switch activity and duty cycle as shown in Equation 5 and plotted as in Figure 3.1.1.

Equation 1 - Energy Stored in an Ideal Capacitor

$$E = \frac{1}{2}CV^2$$

Equation 2 - Energy stored for different voltage levels

$$\frac{1}{2}(3 \times 10^{-12})(80^2) = 19.2nJ$$

$$\frac{1}{2}(3 \times 10^{-12})(20^2) = 1.2nJ$$

$$\frac{1}{2}(3 \times 10^{-12})(10^2) = .3nJ$$

Equation 3 - Energy stored in Positive Pull-Down

$$(19.2nJ + 1.2nJ + 19.2nJ) \times (\#cycles)$$

Equation 4 - Energy stored in Hold-Down

$$(1.2nJ + .3nJ) \times (\#flips)$$

Equation 5 - Normalized Ideal Power Expression for RF MEMS Microswitch

$$Power = (6.6nJ) \times (\#cycles) + (((1 - PullDownTime)) / HoldDownTime) \times (1.5nJ) \times (DutyCycle)$$

APPENDIX B

COMMERCIALLY AVAILABLE TECHNOLOGIES

Many commercially available technologies for the bias of RF MEMS are solutions designed for use in the development stage and processes of MEMS. A common solution used for testing is a high speed, high voltage amplifier with a general purpose waveform generator. This allows great flexibility on the bench. A listing of commercially available high voltage amplifiers is shown in Table B.1. Besides bench top units, integrated op-amps can be purchased. Some of these are listed in Table B.2.

Manufacturer	Model	Voltage Level (V)	Bandwidth (MHz)	Slew Rate (V/ μ s)
Falco Systems	WMA-300	± 150	5	2000
TREK	PZD350	± 350	.15	500
TEGAM	2340	± 200	2	250

Table B.1 - Commercially Available High Voltage Amplifiers

Manufacturer	Model	Voltage Level (V)	Gain-Bandwidth (MHz)	Slew Rate (V/ μ s)
Burr-Brown	3584	± 150	50	150
M.S. Kennedy	601	± 110	200	3000
Supertex	HV254	+250	.25	3
Apex	PA85	± 225	100	1000

Table B.2 - Commercially Available Op-Amps

There are also some nonlinear IC's available that could potentially be used as well. Many of these are typically used as pulsers in medical ultrasound equipment. The Supertex HV739 is a good example. It can deliver a positive and

negative 100 V pulse with fast (50 ns) rise and fall times. Another similar example would be a high voltage analog switch. Examples include the Clare CPC7220 and the Supertex HV2201. Both devices are arrays of semiconductor switches that will create a low resistance connection between two terminals from a low voltage control signal. Either of these options could be used to create a system in which several high voltage levels were switched to create a bias waveform.

APPENDIX C

HIGH VOLTAGE GENERATION OPTIONS

C.1 Linear Regulator

A linear regulator is one of the most common voltage regulation devices. It can essentially be thought of as a voltage controlled current source. The current source is slaved to a reference voltage and the voltage feedback from the output. Any difference in these voltages causes the current source to deliver more or less current to the load. Commercial standalone regulators are typically made in a bipolar process such as described in [17]. There are also options in CMOS processes that can essentially use an op-amp for the same function as described in [18]. These devices work well; however, they cannot generate a voltage higher than the given input voltage.

To generate the voltages necessary for the bias generator application, a high voltage linear regulator would be needed that could regulate a voltage of 80 V from a source voltage greater than 80 V. Since the RF MEMS microswitch is a nearly pure capacitive load, there would be significant current losses due to quiescent current flowing through the regulator when the switch was open and also in the time after charging had occurred (much of the hold-down cycle). The regulator does typically provide a stiff voltage reference that will source or sink

current to keep the voltage constant. This is a necessary condition when dealing with a load that is purely capacitive.

C.2 Charge Pump

A charge pump is a widely used DC-DC converter circuit topology. The basic idea of a charge pump is to use capacitors to either step the voltage up or divide it down. In the step-up form there are two main topologies. The first one is known as a Dickson pump and is shown in Figure C.1. Here non-overlapping clocks ϕ and ϕ_{not} are used to alternately push the voltage up at each node in the chain of diodes by using the capacitor as a “bucket” of charge. Since the current can only flow one way through the diode, it charges up the next capacitor, which due to the out of phase clocks, is at its lowest potential state. This process can continue for many stages.

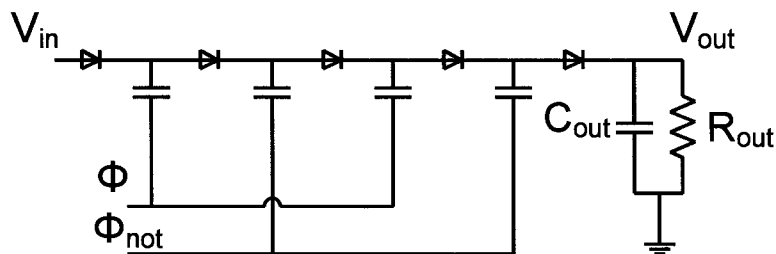


Figure C.1 – Dickson charge pump (Step Up)

The Dickson pump can in theory be used to generate any voltage from any voltage. In practice there are losses for each stage added. There are losses due to the diode drop and diode resistance, as well as parasitic losses in each capacitor, that form capacitive dividers at the top electrode of each capacitor. The topology is serial, thus leading to a multiplying effect of the losses through

the pump. After only several stages, the efficiency drops rapidly. A thorough analysis and explanation of Dickson charge pumps can be found in [19].

The second major charge pump topology is known as a voltage doubler. It is shown in Figure C.2. The capacitor C_d is charged to the input voltage. The non-overlapping clocks then reverse the connections to the capacitor, switching the bottom plate reference from ground to V_{in} and the output from V_{in} to V_{out} . The charge in C_d then flows into the output at double the input potential. In a single stage it operates much like the Dickson topology, but when cascaded the voltage is doubled on each successive stage. Exponential voltage increases are possible compared with the linear increases in the Dickson pump. Problems occur in the treatment of the switches as ideal. The pump can only operate if the voltages across all the transistors are within their operational limits. Use of power transistors, such as DMOS, present new challenges since level-shifted gate voltages must be generated that track the output voltage of each transistor. DMOS devices also are highly resistive, thus generating large losses. Consequently most doublers are limited to low voltage applications. A complete comparison of different charge pump designs can be found in [20].

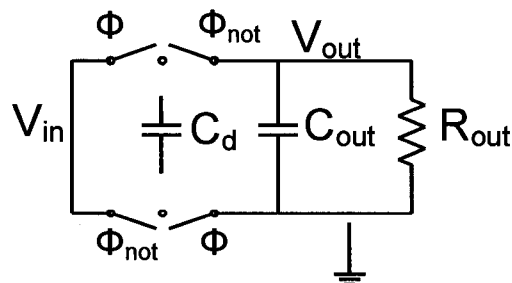


Figure C.2 - Voltage Doubler

C.3 Buck-Boost

The Buck-Boost converter is a combination of a Buck, or voltage step-down converter, with a Boost or voltage step-up converter. The circuit configurations of all three are very similar and operate under the same principle. A schematic can be found in Figure C.3. When the switch is closed, current flows into the inductor and the diode becomes reverse biased. Assuming it has been previously charged, the capacitor supplies energy to the load R_{out} . When the switch is open, the diode becomes forward biased and connects the inductor to the load, thereby transferring its energy to the capacitor and resistor. Depending on the sizing of the inductor, the switching frequency and the load resistance the magnitude of the voltage at the output can be larger or smaller than that at the input.

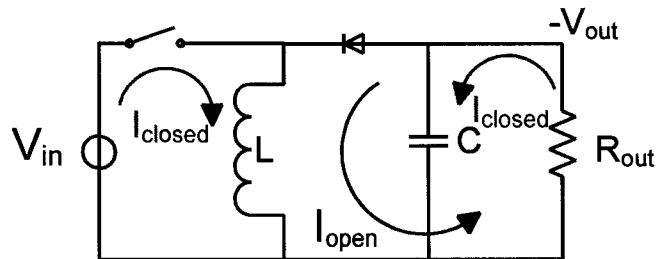


Figure C.3 - Buck-Boost Converter

The Buck-Boost converter provides the advantages of readily and efficiently converting voltages. It also is a simple circuit requiring few (only 5) circuit elements. It lacks the ability to be fully integrated due to the small size inductors typically available in most integrated processes. In most designs the inductor and capacitor are large and external elements. Like the charge pump designs, it also needs to have a regulation stage in order to smooth out the fluctuations in voltage.